PCB Renewal: Iterative Reuse of PCB Substrates for Sustainable Electronic Making

Zeyu Yan
Department of Computer Science
University Of Maryland
College Park, Maryland, USA
zeyuy@umd.edu

Advait Vartak
Department of Computer Science
University of Maryland
College Park, Maryland, USA
avartak@terpmail.umd.edu

Jiasheng Li
Department of Computer Science
University of Maryland
College Park, Maryland, USA
jsli@umd.edu

Zining Zhang
Department of Computer Science
University of Maryland
College Park, Maryland, USA
znzhang@umd.edu

Huaishu Peng
Department of Computer Science
University of Maryland
College Park, Maryland, USA
huaishu@umd.edu

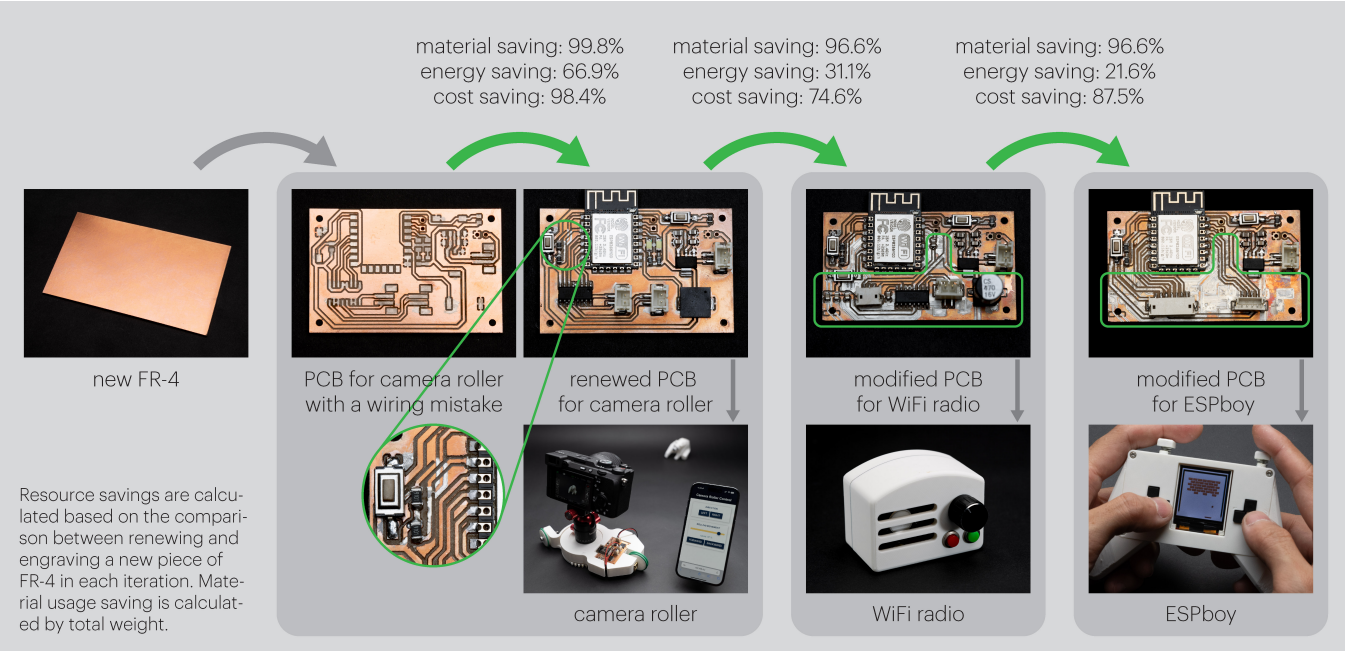

Figure 1: PCB Renewal: a single piece of FR-4 was renewed for four iterations across three projects, significantly reducing resource consumption compared to engraving new circuits for each iteration.

Abstract

PCB (printed circuit board) substrates are often single-use, leading to material waste in electronics making. We introduce PCB Renewal, a novel technique that "erases" and "reconfigures" PCB traces by selectively depositing conductive epoxy onto outdated areas, transforming isolated paths into conductive planes that support new traces. We present the PCB Renewal workflow, evaluate its electrical performance and mechanical durability, and model its sustainability impact, including material usage, cost, energy consumption, and time savings. We develop a software plug-in that guides epoxy deposition, generates updated PCB profiles, and calculates resource usage. To demonstrate PCB Renewal 's effectiveness and versatility, we repurpose a single PCB across four design iterations spanning three projects: a camera roller, a WiFi radio, and an ESPboy game console. We also show how an outsourced double-layer PCB can be reconfigured, transforming it from an LED watch to an interactive cat toy. The paper concludes with limitations and future directions.

CHI '25, Yokohama, Japan

ACM ISBN 979-8-4007-1394-1/25/04
https://doi.org/10.1145/3706598.3714276

CCS Concepts

• **Social and professional topics** → **Sustainability**; • **Hardware** → **Printed circuit boards**; • **Human-centered computing** → *Systems and tools for interaction design.*

Keywords

PCB Prototyping, Sustainability, Reuse, Renewal, Fabrication

ACM Reference Format:

Zeyu Yan, Advait Vartak, Jiasheng Li, Zining Zhang, and Huaishu Peng. 2025. PCB Renewal: Iterative Reuse of PCB Substrates for Sustainable Electronic Making. In *CHI Conference on Human Factors in Computing Systems (CHI '25), April 26–May 01, 2025, Yokohama, Japan.* ACM, New York, NY, USA, 18 pages. https://doi.org/10.1145/3706598.3714276

1 Introduction

Printed circuit boards (PCBs) are critical components in nearly all electronic devices. However, the obsolescence of PCBs, from their design process to end-of-life disposal, has become an increasingly significant source of electronic waste (e-waste).

The design of a functional PCB typically involves multiple stages, including software simulation, circuit validation (e.g., via breadboarding), and prototyping with custom PCB batches. While the simulation and breadboard validation phases generate minimal e-waste—since engineers test functionality digitally or reconfigure reusable components like breakout boards, through-hole electronics, and jumper wires—the subsequent PCB prototyping stage inevitably contributes to e-waste production.

PCBs are made using a subtractive fabrication method, where copper layers are permanently etched from laminated substrates (e.g., FR-4, a fiberglass-reinforced epoxy), making the process *inherently irreversible*. During PCB prototyping, minor errors—such as flaws in electronic design automation (EDA) schematics or mismatches between PCB dimensions and their housing—are often discovered. While these issues may be small and easily corrected digitally, they are physically embedded into the substrates, rendering the entire prototype (or batches, if outsourced to factories) unusable. This necessitates the repeated production of new PCBs, while discarded ones contribute to e-waste.

Mass-produced PCBs further exacerbate the e-waste problem when devices reach the end of their life cycle. In 2022, less than 23% of globally generated e-waste was formally collected and recycled. Even when PCBs are recycled, their inherently irreversible fabrication process forces them into centralized waste streams, where they are processed indiscriminately. As a result, they are rarely repaired, repurposed, or reused—even though many PCBs and their substrates remain functional [4].

These e-waste challenges have garnered attention in the HCI community, as evidenced by sustainable making and unmaking workshops at UIST and CHI [56, 66], and a dedicated TOCHI special issue [60]. Recent work has also called for a reimagining of end-users' roles, emphasizing their potential not only as consumers but also as active participants in PCB recycling and reuse [43]. Additionally, researchers have advocated for the development of new processes, tools, and infrastructure to address e-waste and promote sustainable practices [67].

In this paper, we contribute to sustainable PCB practices by proposing a *reversible* PCB substrate fabrication process that enables the "erasure" and "reconfiguration" of copper layouts. Central to this process is the additive restoration of removed copper areas using conductive fillers, such as conductive epoxy, to renew the PCB substrate for fresh trace patterns. Analogous to a correction pen overwriting mistakes on paper, our approach extends the lifespan of PCB substrates by enabling physical re-editing to correct design errors or remove obsolete traces. This transforms what would otherwise become e-waste into new designs (Figure 1). We call this approach PCB Renewal.

In the remainder of this paper, we introduce the workflow of PCB Renewal, providing a detailed examination of conductive filler materials and the key fabrication processes involved in the renewal of the commonly used PCB substrate FR-4. We validate our approach through a series of experiments that evaluate key electrical parameters, including conductivity, current capacity, solder joint durability, and the number of renewal iterations a single FR-4 board can undergo. These experiments demonstrate that the renewed substrate exhibits electrical performance comparable to that of raw FR-4. To assess the sustainability impact of PCB Renewal, we present a quantitative analysis model that compares PCB Renewal with the fabrication of new circuits using raw FR-4. This model includes estimates of material usage, cost, time, and energy consumption. To help end-users incorporate PCB Renewal into their workflow to save PCB substrates during prototyping or repurpose PCB designs in general, we develop an EDA software plug-in. This plug-in allows end users to update a circuit design with changes visualized across iterations, evaluate the sustainability impact of specific renewed designs, and generate the fabrication profiles required for renewal.

PCB Renewal can be applied to PCBs fabricated either in-house or through outsourcing. To demonstrate its versatility, we provide a detailed account of a single PCB reused across four in-house design iterations for three distinct projects: a wireless camera roller, a WiFi radio, and an ESPboy game console. Additionally, we demonstrate that an outsourced double-layer PCB, originally made for an LED watch, can be renewed and repurposed for a cat toy using the PCB Renewal process. We report the sustainability impact of each design iteration for all examples. We conclude with a discussion on the limitations of PCB Renewal and its potential future directions.

2 Related Work

Our work is inspired by a substantial body of prior research in sustainable human-computer interaction (SHCI), methods for recycling or reusing electronic and electronic waste, as well as technical explorations in PCB substrate repair and renewal.

2.1 Sustainability in HCI: Making and Prototyping

The notion of Sustainable Interaction Design (SID) was introduced by Blevis [9] over a decade ago, providing a foundational framework for addressing environmental impacts and human behavior in the design of interactive technologies. This concept has since evolved into the broader field of SHCI.

Early discussions in SHCI often centered on mobile applications and their influence on end-users' daily behaviors, such as reducing energy consumption through persuasive computing [24, 25]. More recently, attention has shifted to the environmental impact of making and physical prototyping [56, 66], driven by the democratization of personal fabrication tools and the growing maker movement [31, 55].

Several studies have explored end-users' (creative) approaches to engaging with wasted physical materials in daily activities. For example, Yan et al. [67] have presented a qualitative research that maps out the sustainability practices, challenges and opportunities in modern makerspace setups and have called for new tools and infrastructure to support making sustainably. Kim and Paulos [36] have proposed a reuse composition framework, based on online surveys and observations, to inspire the creative reuse of material waste. Dew and Rosner [21] have conducted design explorations that examine how designers conceptualize, manage, and rework waste materials in educational makerspaces. Similarly, Maestri and Wakkary [45] have studied the intersection of repair and creativity within household settings. These ideas have since evolved into broader concepts, such as unmaking [58], uncrafting [50], and unfabricating [65], which employ speculative or participatory design lenses to explore the afterlife of objects and materials.

Alongside the exploration of reusing daily waste, HCI researchers have begun investigating the use of decomposable and biodegradable materials in making. For example, several projects have proposed using edible materials [11, 57] or substances derived from food waste [54] as construction materials for molding and 3D printing. Microbe-based materials, such as yeast [7] and fungi [34, 62], as well as biomaterials derived from living organisms, including algae [6] and cellulose-based fibers [27, 37], have also been proposed as building materials for the prototyping of interactive devices.

In addition, new fabrication processes and tools have been developed to support more sustainable making practices. For example, Filament Wiring [20] and Substiports [63] introduce alternative fabrication pipelines that repurpose wasted 3D printing filament or failed prints for new designs. EcoThreads [74] and Desktop Biofibers Spinning [40] have developed new machines and processes to make water-dissolvable yarns easily accessible for sustainable textile applications.

Our work is greatly inspired by the aforementioned advancements in sustainable making, with a specific focus on the processes involved in PCB making. As discussed in the introduction, PCBs are among the largest contributors to e-waste. Our work aims to reduce this environmental impact.

2.2 Supporting the Reuse and Recycling of Electronics

E-waste recycling requires interdisciplinary research and collaborative practices.

In the electronics management industry, the primarily focus is on infrastructure and large-scale processes that can extract raw materials from PCB scrap. For example, chemical and mechanical techniques are used to recover valuable materials, including refractory metals and elements of the platinum group found in standard PCB waste [29, 48]. Although effective, these industrial and centralized approaches void the opportunities for PCBs that might be repurposed, repaired, or reused, and they may fall short as more individuals become involved in creating electronics through the democratization of making tools.

Recent HCI literature points out that many end users are no longer just consumers of physical artifacts but also their creators. Consequently, they bear greater responsibility for managing the material waste generated during the individual making process [43, 67]. In this context, much of the HCI research focuses on promoting the reuse and recycling of electronics at the individual level. For example, the CurveBoards project [73] proposes a custom-shaped breadboard design that is versatile for rapid prototyping with form-specific requirements. CircuitGlue [38] reduces waste in prototyping by allowing easy integration and reuse of off-the-shelf components. SolderlessPCB [68] demonstrates a pressure-based PCB assembly method using 3D printed or CNC-made housings, allowing easy disassembly and reuse of surface-mounted components. ecoEDA [42] shows how interactive circuit design software, by integrating early-stage suggestions for utilizing recyclable electronic components from stock PCBs, can facilitate the reuse of electronics throughout the design process.

New, more environmentally friendly PCB materials and compositions have also been explored. For example, transesterification vitrimers have been proposed as PCB substrate materials, which can be recycled through polymer swelling, achieving a 98% polymer recovery [71]. Several studies have investigated PCB substrates based on paper [15, 35, 64], wood [33], and water-soluble materials [2, 8, 26]. Water-soluble materials are particularly interesting in the context of sustainable electronics, as their degrading processes are controllable. This enables the creation of transient electronic prototypes [30, 70] with programmable lifespans, simplifying the recycling of materials once they are no longer needed [16, 17, 59].

Our work also aims to reduce material waste from PCBs. However, instead of focusing on new materials that may not be readily available to many, we seek to improve the workflow of the existing FR-4 substrate-based PCB manufacturing process. Our approach relies solely on off-the-shelf conductive epoxy and CNC engraving machines, which have become more affordable and widely available in makerspaces. As a result, our method has the potential to be adopted at scale.

2.3 PCB Substrate Repair and Renewal

Although PCBs are generally considered irreversible, several solutions have been proposed to repair minor errors or shorts. For example, jumper wires can restore electrical continuity between disconnected points [18], while conductive ink pens enable temporary, ad-hoc circuit repairs [13]. However, these methods are primarily effective for minor fixes, such as bridging gaps over short distances, and are not suitable for more complex repairs that require removing multiple conductors or altering component footprints and placements.

Several studies have investigated methods for fixing regional circuit errors. For example, Chen et al. [14] have developed a local electroplating technique to repair constrictions in copper traces.

Lim et al. [41] have proposed repairing broken circuit traces using reduced graphene oxide on a laser direct writing platform. Lange [39] has demonstrated the use of UV and IR lasers to trim fuzzy edges of conductor shapes on PCBs, reducing the defect rates in PCB products. However, these approaches focus on repairing defects in PCB traces rather than addressing circuit design errors through rerouting or editing existing circuits.

Prior to our work, preliminary explorations have demonstrated the potential of using conductive filler deposition to modify or repair existing circuit diagrams on substrates. For example, Self-healing UI [51] has introduced a composite material capable of autonomously repairing circuit wiring made of multiwall carbon nanotubes by leveraging the dynamic cross-linking properties of polyborosiloxane polymers. However, carbon nanotubes are hazardous and require specialized handling, and circuits made with this composite are limited to low-fidelity prototypes. Circuit Eraser [52] has proposed using a standard eraser to remove circuit traces printed with conductive ink, facilitating rapid iteration of circuit design. Silver Tape [15] enables circuit trace repair via tape transfer of inkjet-printed silver ink. Furthermore, Marghescu et al. [22] and Drumea et al. [46] have evaluated the current-carrying capacity of sectional circuit traces made with nickel and silver paste, confirming the potential of PCB repair using conductive pastes.

Building upon previous research, we investigate the additive method of paste deposition as an alternative to the conventional subtractive PCB engraving process. This approach enables the renewal of circuit boards originally fabricated using methods such as CNC engraving or photochemical etching. Furthermore, our method enables the editing of large conductive areas, allowing an existing PCB designed for a specific purpose to be repurposed for different projects. This, therefore, increases the opportunity to reuse otherwise wasted PCBs, reducing unnecessary e-waste.

3 PCB Renewal

PCB Renewal is a simple yet effective approach to repurposing PCB substrates that would otherwise be discarded. It helps reduce e-waste during PCB prototyping by enabling the correction of design errors, such as incorrect circuit trace connections or component misplacements, directly on faulty PCBs. Additionally, PCB Renewal facilitates the reuse of obsolete outsourced PCBs, particularly open-source designs. By updating trace areas that are no longer needed, it provides retired PCBs with new functionalities.

As illustrated in Figure 2, the core of the renewal process is the selective deposition of conductive filler material into isolation grooves to "erase" existing circuit traces or pads, allowing new conductive traces to be re-engraved. PCB Renewal assumes access to conductive epoxy as a filler material and a CNC or laser-cutting machine for modifying the PCB substrate. To support this process, an EDA software plug-in (Section 6) has been developed to compare new circuit designs with the existing layout and apply selective modifications only where necessary.

By preserving existing copper conductors and much of the fiberglass substrate, PCB Renewal significantly reduces material waste, manufacturing costs, and energy consumption while maintaining a fabrication time comparable to producing a new PCB. Its core refilling and re-engraving processes are independent of board type, making it suitable for both in-house and factory-made PCBs, as well as single- and double-sided designs, though creating new vias for double-sided PCBs requires manual effort.

In the following sections, we use in-house PCBs with FR-4 substrates to explore key considerations and experiments related to PCB Renewal. In Section 7, we showcase examples of repairing and repurposing PCB substrates fabricated both in-house and through outsourced manufacturers.

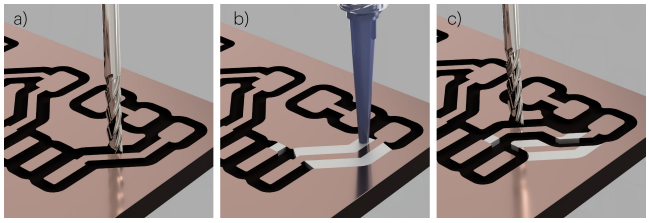

Figure 2: PCB Renewal principle illustration: a) initial PCB engraved, b) selectively depositing conductive filler into isolation grooves, c) re-engraving new circuit trace.

3.1 Material

The key to PCB Renewal is refilling the isolation grooves of a PCB substrate to restore the conductive plane. This requires the conductive filler material to exhibit high conductivity, comparable to that of the original copper conductors. In addition, the filler material must form a robust bond with the PCB substrate while possessing physical properties that allow for controlled and precise deposition.

Our search for suitable materials began with solder wire and solder paste, widely accessible conductive materials known for their excellent electrical conductivity. However, these materials are designed primarily to create strong metal-to-metal bonds between electronic components and copper circuit pads. Specifically, they exhibit high surface tension in their liquid state and are formulated to form metallurgical bonds exclusively with unoxidized metal surfaces [32]. As fiberglass is inert to metallurgical bonding, solder tends to flow toward the copper surface rather than settling in isolation grooves.

In contrast to solder, conductive epoxy products are widely used in PCB screen printing and plotting processes. These polymer-based conductive epoxies exhibit high electrical conductivity for circuit traces and cure to a glassy state rather than transition to a high-surface-tension liquid, as is the case with solder. This property allows for uniform bonding to both metallic and inert substrates.

Conductive epoxies are formulated with a variety of fillers, including silver, nickel, copper, carbon, and graphene. Notably, silver-based epoxies are available in single-part formulations that require no mixing and do not need specialized curing treatments, such as formic acid fumes, laser processing, or flash lamp exposure. Therefore, we surveyed a range of off-the-shelf, single-part, thermoset silver-based conductive epoxies, as shown in Table 1.

We considered four technical criteria when selecting the appropriate conductive epoxy. First, the curing temperature must not exceed the maximum operating temperature of commonly used

Table 1: Silver Epoxies Surveyed

Name (code)	Volume resistance (μΩ · cm)	Viscosity (Pa · s)	Curing time (min)	Curing temp (°C)
Voltera Conductor 3	127	not reported	15	170
AA-duct 2979	30	65	15	150
ACI FS0142	6	15	15	150
DM-SIP-3072S	7.5	10	10	150
Metalon® HPS-021LV	10.4	2.6	30	150

PCB substrates such as FR-4 (150 °C for Tg150 FR-4). Second, we prioritized materials with lower volume resistivity to maximize the current-carrying capacity of the traces passing through epoxy-filled areas. Therefore, we targeted a volume resistivity of the conductive epoxy that does not exceed 10 μΩ · cm, which is within the same order of magnitude as copper. Third, the viscosity of the material at room temperature is critical. Through empirical testing, we observed that excessive viscosity hinders efficient flow and proper filling of the filler material in tiny engraved grooves, resulting in poor mechanical bonding and unreliable electrical connections (Figure 3a). On the other hand, excessively low viscosity causes the epoxy to flow away from the intended deposition areas or spread unevenly along the engraved grooves (Figure 3b). Based on our experiments, we determined that a room-temperature viscosity of approximately 10-15 Pa · s satisfies our requirements. Fourth, to simplify the filler deposition process, we exclusively considered single-part conductive epoxy. This choice eliminates the need for mixing and minimizes material waste from residual mixtures.

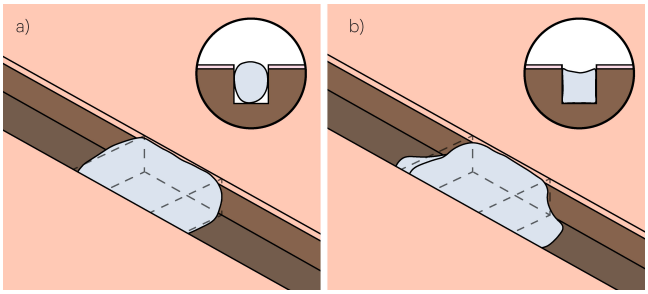

Figure 3: Illustration of conductive epoxy behavior at different viscosities: a) excessively high viscosity, b) excessively low viscosity.

These criteria led to the selection of two materials from the tested silver-based conductive epoxies: ACI FS0142 and DM-SIP-3072S. Based on material availability at the site the research was conducted, ACI FS0142 was chosen for all samples in this study unless otherwise noted. This heat-cured, single-part epoxy is specifically designed for PCB screen printing, has a viscosity of 15 Pa · s at room temperature, and cures at 150 °C in 15 minutes.

Note that the goal of this search was to identify one conductive filler that meets our design requirements for PCB Renewal. This survey is not exhaustive, and other materials may perform equally well or better.

3.2 Fabrication Pipeline

The fabrication pipeline for renewing a PCB consists of four main steps: desoldering, depositing, curing, and engraving. We illustrate this process (Figure 4) by correcting an in-house PCB with a trace that was incorrectly connected due to a design error. Specifically, the example circuit includes an ATtiny85, a toggle switch, a JST connector, an LED, and a resistor that was mistakenly connected to the wrong pin of the ATtiny. During the renewal process, the incorrect trace is rerouted to connect to the correct pin, which is programmed to control the LED's blinking. As noted earlier, while we used a single-sided, CNC-milled PCB as the walkthrough example, our method is applicable to double-sided PCBs and those manufactured through outsourcing.

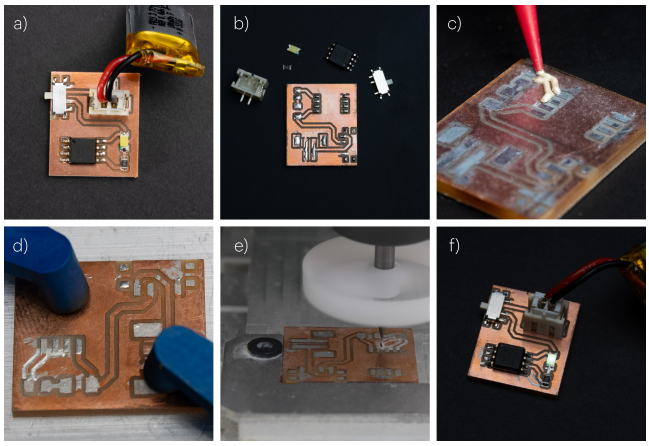

Figure 4: Fabrication workflow: a) old board, b) desoldering, c) manual epoxy deposition with a stencil,, d) epoxy curing, e) engraving new traces, f) new functional PCB with a modified trace.

Step 1 — Desoldering: PCB Renewal begins with desoldering the components from the old PCB (Figure 4a-b). This step is essential because material deposition, curing, and new trace engraving can only be performed safely on a bare board. Although components far from affected areas might theoretically remain in place during small, localized modifications, we recommend fully removing all components. The heat curing process often reaches the solder's soaking temperature range, potentially compromising connection performance if components are left on the board.

Step 2 — Depositing: After desoldering, conductive epoxy is deposited into the engraved grooves to be restored. This process can

be performed manually, similar to applying solder paste, or using a CNC machine with a paste extruder add-on. In our case, we use a syringe with a 23-gauge tapered blunt tip to manually deposit the conductive epoxy. An optional stencil can be generated from our software plugin (see Section 6). The stencil profile features openings that align with the isolation areas to be restored (Figure 4c). When applying epoxy, it is important to ensure that there are no visible gaps between the epoxy and the adjacent copper to prevent open circuit spots on the updated board. Excess material can be removed manually before peeling the stencil off the board or with a CNC milling machine after the epoxy has cured.

Step 3 — Curing: Once the epoxy is applied, the board is cured by placing it in a convection oven or on a soldering hot plate. We cure the epoxy at 150 °C for 15 minutes using a hot plate (see Figure 4d).

Step 4 — Engraving: After curing, the board is allowed to cool to room temperature before being placed on the CNC milling machine to engrave the updated traces (Figure 4e). An alignment bracket is used to position the bottom-left corner of the board at the machine origin. The engraving profile, obtained from the software plug-in, is then imported and aligned with the machine origin in the CNC control software. Since cured silver epoxy is softer than the FR-4 substrate, the engraving Gerber file and G-code can be generated using the same tooling and settings as a standard FR-4 PCB. In this project, all samples are engraved using a Bantam Tools desktop CNC milling machine [5].

4 Performance Characterization

As PCB Renewal introduces conductive materials other than copper for creating new PCB traces, it is essential to evaluate its electrical and mechanical performance to determine whether it can serve as a reliable iterative PCB making approach. To this end, this section outlines a series of experiments designed to evaluate PCB Renewal 's performance, focusing on factors such as fabrication resolution in epoxy areas, electrical conductivity at copper-epoxy intersections, the current-carrying capacity of the traces, soldering performance, and the maximum number of renewal cycles achievable with this method.

4.1 Fabrication Resolution

In CNC-engraved PCBs, the bonding strength between the conductive and dielectric layers is inversely related to the minimum trace width. Thinner traces are more prone to delamination from the fiberglass substrate. Consumer-grade CNC milling machines generally recommend trace widths of at least 10 mil (where 1 mil is one-thousandth of an inch or 0.0254 mm) [1]. Renewed PCBs, which bond conductive epoxy to the fiberglass substrate through heat curing, may exhibit different bonding strengths compared to copper in standard FR-4. To determine the minimal engravable trace width for renewed PCBs, we conducted an experiment using varying trace widths in a conductive epoxy pour.

We began by engraving a rectangular area on an FR-4 board to a depth of 0.15 mm, which is the typical depth for creating PCBs with desktop CNC machines. The engraved area was then filled with conductive epoxy, leveled to flush with the surrounding copper, and cured on a hot plate. Once the epoxy was fully cured, 10 mm circuit traces with contact pads at both ends were engraved directly onto the epoxy surface. The trace widths ranged from 2 to 20 mil, increasing in 2-mil increments. Each width was tested three times, with the results shown in Figure 5. Traces narrower than 6 mil failed in all three attempts, while those 6 mil and above consistently succeeded, aligning with the recommended minimum trace width for CNC copper circuits. In practice, we recommend designing circuit traces with the widest width that a design can accommodate to ensure optimal reliability.

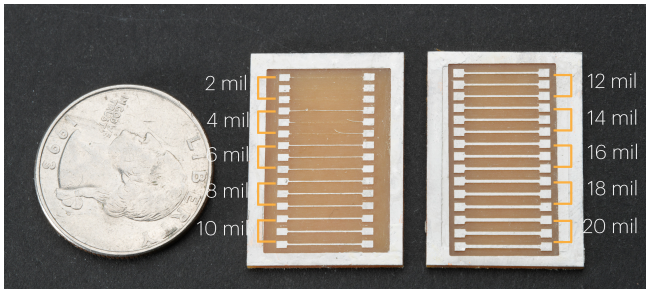

Figure 5: Fabrication resolution: trace engraving was attempted on a conductive epoxy pour at various trace widths.

4.2 Electrical Conductivity

A renewed PCB contains circuit traces made of silver epoxy or a hybrid of silver epoxy and copper. To understand how variations in material composition affect trace conductivity, we conducted two sets of experiments.

4.2.1 Conductive Epoxy Trace Conductivity. To evaluate the conductivity performance of the silver epoxy traces, we used traces with widths of 6 mil and above from the samples fabricated in Section 4.1. Since the actual width of the engraved traces is influenced by manufacturing errors, we measured the actual trace width using a microscope stage, interpolating measurements to 0.1 mil. The resistance of each trace was measured using a Keysight 3446SECU digital multimeter. The average measured trace width and resistance for each specified trace width were calculated from measurements taken across three individual traces. The average trace widths were rounded to two decimal places, while the average resistance values were rounded to three decimal places, as presented in Table 2.

Table 2: Conductivity of Conductive Epoxy Traces

Nominal width (mil)	Measured width (mil)	Resistance (Ω)
6	3.47	0.287
8	6.83	0.134
10	9.50	0.136
12	10.93	0.108
14	12.20	0.105
16	14.37	0.102
18	16.33	0.101
20	18.03	0.088

As shown in the table, all the traces exhibit a resistance of less than 0.3 Ω per centimeter, with the majority below 0.15 Ω, making them suitable for implementing most low-frequency DC circuit functionalities.

4.2.2 Material Interface Conductivity. PCB Renewal creates bonding seams between copper and epoxy, through which current flows. To assess the reliability of these seams, we conducted an experiment simulating real-world conditions to evaluate the quality of the connections at these points.

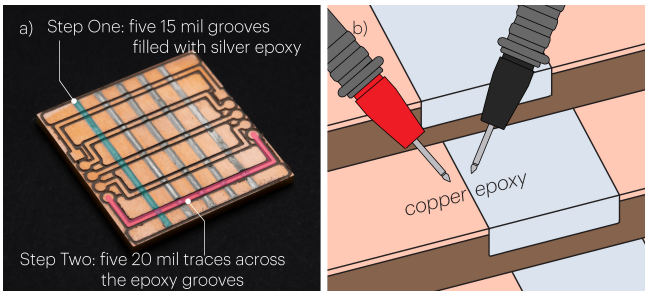

Figure 6: Material interface experiment: a) hybrid material traces (20 mil wide), b) illustration of measurement points.

We began with five parallel grooves, each 15 mil wide—the smallest typical square end mill diameter used for circuit boards with desktop CNC milling machines. Then, conductive epoxy was deposited in each groove. After curing, we engraved five 20 mil traces perpendicular to the grooves. As a result, each trace contained 10 epoxy-copper bonding seams for investigation (Figure 6a). We measured the resistance of all 50 seams using a Keysight 3446SECU digital multimeter, probing as closely as possible to both sides of each seam (Figure 6). The seams consistently exhibited a resistance of 0.146 Ω with a standard deviation of 0.0345 Ω, demonstrating that hybrid-material circuit traces can achieve electrical performance comparable to pure copper traces.

4.2.3 Current Capacity. Introducing an additional material into circuit trace formation can result in localized thermal accumulation due to uneven resistance. To evaluate the performance of conductive epoxy traces under high-current conditions, we tested the current-carrying capacity of the traces fabricated in Sections 4.1 and 4.2.2. Fixed currents of 1 A, 3 A, and 5 A were applied to each trace using a bench power supply, and the temperature was monitored with a thermal camera. All experiments were conducted at a room temperature of 22 °C.

We observed that the temperature increase of all traces remained below 23 °C under a current of 1 A (Figure 7a). When subjected to 3 A, 6-mil traces fused within three seconds, while the remaining traces exhibited a maximum temperature rise of 66 °C (Figure 7b). Under a 5 A load, traces narrower than 20 mils fused in five seconds. However, the 20-mil traces remained functional, with a temperature increase below 120 °C, which is within the 150 °C Tg rating of the FR-4 board (Figure 7c). These results indicate that traces produced by our method have sufficient current-carrying capacity for low-current DC signal circuits. For applications requiring currents above 3 A, a minimum trace width of 20 mils is recommended.

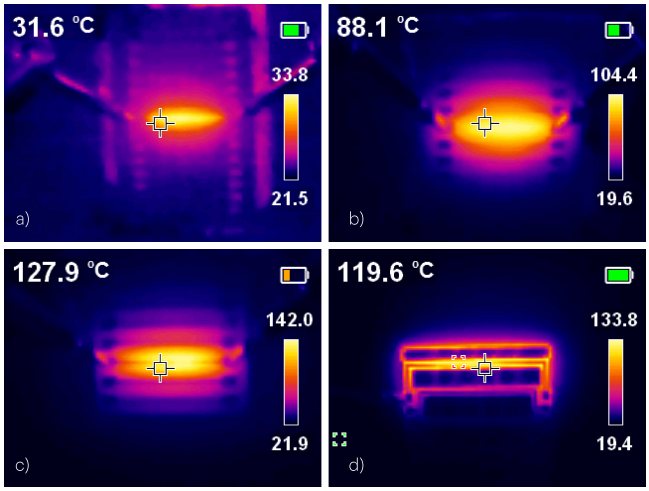

Figure 7: Current capacity experiment–thermal camera images of: a) 6 mil trace under 1A, b) 8 mil trace under 3A, c) 20 mil trace under 5A, d) hybrid material 20 mil trace under 5A.

Furthermore, we observed that the hybrid traces fabricated in Section 4.2.2 exhibited higher temperature increases at the conductive epoxy segments. However, at the same current levels, the temperature rise did not exceed that of traces made entirely from conductive epoxy (Figure 7d).

4.3 Solder Joint Performance

In addition to circuit traces, PCB assemblies must ensure both conductivity and mechanical durability at solder joints. The renewed PCB design will likely incorporate solder pads partially or entirely made of silver epoxy. We investigated the conductivity and strength of the solder joint using 0805 resistors and their corresponding solder pads. Following a process similar to that in Section 4.1, we fabricated silver epoxy-based traces with solder pads designed for 0805 resistors. The resistors were soldered (Figure 8a) to six samples using low-temperature solder paste [12], as recommended by the silver epoxy manufacturer. Three samples were soldered using a hot plate, while the other three were soldered with a hot air blower.

The resistance of the solder joint was measured by probing the solder pad and the corresponding resistor terminal, using a 3446SECU digital multimeter (Figure 8b). For comparison, we fabricated another set of samples on copper substrates with identical trace and pad geometry, soldering 0805 resistors using the same solder paste and soldering methods. For both copper and epoxy pads, the hot air blower and hot plate methods produced similar solder joint resistance (Table 3, rows 1 and 2). The difference in resistance between solder joints on copper and epoxy pads was less than 0.1 Ω, a negligible value that does not affect the functionality of DC or AC signal circuits.

In addition to conductivity, we used the same set of samples to evaluate the strength of the solder joints. Pressure was applied to the soldered resistors at a 30-degree angle (Figure 8c) until they detached from the solder pad. A DFS100 force gauge recorded the peak force value. The samples soldered on epoxy pads broke off with an

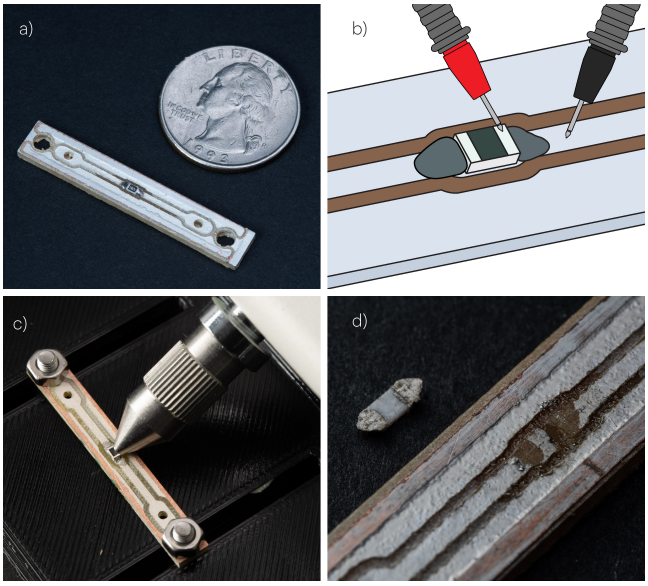

Figure 8: Solder joint experiment: a) an example of a solder joint experiment sample, b) the probing location adopted when measuring solder joint resistance, c) force gauge pressing on the soldered resistor at 30-degree angle, d) epoxy trace failure while the solder joint stays intact.

Table 3: Solder Joint Conductivity and Strength

Solder equipment	Hot plate	Hot air	All samples
Copper conductivity (Ω)	0.17	0.18	0.18
Epoxy conductivity (Ω)	0.22	0.27	0.24
Copper strength (N)	87.67	71.40	79.53
Epoxy strength (N)	39.32	39.21	39.27

average force of 39.27 N, with a standard deviation of 16.16 N, while those soldered on copper pads withstood an average of 79.53 N, with a standard deviation of 17.51 N. Note that for the silver epoxy samples, all break points occurred at the interface between the epoxy layer and the fiberglass, while the solder joints themselves remained intact (Figure 8d). In practice, we recommend avoiding pure silver pads; however, if their use is necessary, increasing the pad size and the width of the connecting traces can help mitigate the risk of delamination. Additionally, during testing, all connection points remained intact and functional, even after multiple drops from a height of 1.5 m.

4.4 Number of Renewal Iterations

In theory, an FR-4 substrate can be renewed indefinitely, provided that the newly engraved grooves consistently and completely remove the previous epoxy at the exact same Z-height. However, in practice, achieving this level of machining precision is not feasible. To successfully renew a PCB, the engraving depth for new traces must be set deeper than the epoxy deposited in the previous iteration, which corresponds to the prior engraving depth. Based on empirical results, we recommend that with each renewal iteration, the cutting depth be at least 0.05 mm deeper than the previous one.

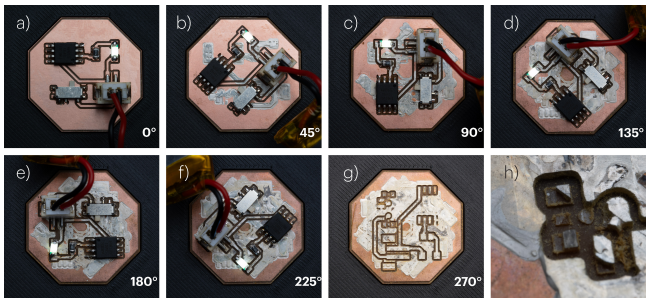

Figure 9: Multi-iteration renewal: a) original circuit, b)-f) second to sixth iteration of circuit modification, each rotated by 45 degrees counter-clockwise, g) the seventh iteration modification with broken traces and pads, h) zoom in view of a broken pad at the interface of copper and epoxy.

As the cutting depth gradually increases with each renewal iteration on an FR-4 board, the trace is positioned progressively higher relative to the bottom of the isolation grooves, making the circuit traces more vulnerable during engraving. We tested the maximum number of renewal iterations using an octagon-shaped PCB. The initial circuit consisted of an ATTiny85, a resistor, an LED, a JST connector for a LiPo battery, and a mini toggle switch. It was originally engraved with an isolation depth of 0.15 mm. The minimum nominal trace width in the circuit was 16 mil (see Figure 9a). For each renewal iteration, we completely erased the old circuit by filling all engraved grooves with conductive epoxy, rotated the board by 45 degrees, and engraved the same circuit with an additional 0.05 mm isolation depth (see Figure 9b-f). We found that the circuit traces remained functional until the seventh iteration, at which point small solder pads and traces began to break (Figure 9g and h).

5 Modeling the Sustainability Impact of PCB Renewal

The primary goal of PCB Renewal is to promote sustainable PCB making by enabling the reuse of PCB substrates. To fully understand its impact, a detailed evaluation is essential. Ideally, a lifecycle assessment (LCA) [28] would be conducted to comprehensively assess the environmental effects of PCB Renewal. However, the variability of each renewal scenario makes it difficult to generalize its impact. For example, if a new circuit design shares no traces with the old one, the renewal process requires a near-complete removal of all old traces and the engraving of entirely new ones. Depending on the PCB size, this may result in a trade-off, where a minor reduction in FR-4 usage is offset by higher energy consumption for epoxy curing, potentially negating any environmental benefits when analyzed quantitatively. Additionally, the lack of LCA data on most silver-based epoxy products further complicates a comprehensive LCA evaluation in practice.

To address this, we adopted the DeltaLCA framework [72] and developed a quantitative comparison model that evaluates key sustainability metrics commonly considered in LCA on a case-by-case

basis. This model estimates and compares material usage, cost, time, and energy consumption between renewing a PCB and fabricating a new one from fresh FR-4. By analyzing these sustainability metrics, end-users can make informed decisions, determining whether renewing a PCB substrate is the more sustainable option or if fabricating a new one is preferable.

Note that while this section focuses on modeling the sustainability impact of PCB Renewal, the model is also integrated into the software plug-in (Section 6). As a result, all modeling parameters—such as deposition path length and trace contour length—can be directly extracted from PCB design profiles, enabling the automatic calculation of PCB Renewal's sustainability impact for each given PCB design.

5.1 Modeling Material Usage and Cost Differences

We chose to estimate material usage based on weight. While weight alone does not fully capture the material trade-offs between a PCB manufactured using the renewal approach and one made with new substrate, it provides the most practical basis for comparison, given the lack of comprehensive carbon footprint data for most silver-based conductive epoxies. In PCB Renewal, users are free to select any homemade or commercially available conductive filler following our guidelines. However, variations in the filler's composition, manufacturing process, shipping distance, curing conditions, and cured material properties, along with other relevant factors, can significantly influence environmental impact metrics, including but not limited to carbon emissions, energy footprint, and toxicity. For example, the energy footprint associated with mining and producing different metal elements used in conductive materials can vary by several orders of magnitude [61]. Given these uncertainties, we provide material usage data in terms of weight as a reliable and conservative basis for further environmental impact modeling. This approach ensures consistency and prevents both overestimation and underestimation of the environmental implications of adopting PCB Renewal.

For PCB Renewal, the primary new materials introduced are conductive epoxy and, optionally, a deposition stencil sheet. The weight of epoxy required (M_e) can be estimated by multiplying the area of the isolation grooves to be filled (A_g) by the depth of the grooves from the previous engraving iteration (d) and the epoxy density (ρ_e). We offset the deposition depth by 0.1 mm by default to account for excess material. This parameter can be adjusted based on actual deposition needs. The area of the stencil sheet (A_s) corresponds to the surface area of the previous board design (A_{b_old}).

$$M_e = \rho_e A_g d$$
$$A_s = A_{b\_old}$$

When calculating material usage for engraving a circuit on a new substrate, neither epoxy nor stencil material is involved. Instead, a fresh piece of FR-4 is used, with an area (A_{FR-4}) that matches the new board design (A_{b_new}).

$$A_{FR-4} = A_{b\_new}$$

We calculate the cost difference between the two methods (denoted as P) based on the unit prices (p_u) of each raw material and the estimated material usage.

$$P_{delta} = M_e p_{u\_e} + A_s p_{u\_s} - A_{FR-4} p_{u\_FR-4}$$

A negative value indicates monetary savings when using PCB Renewal, while a positive value indicates additional costs. Disposable hardware and equipment, such as tooling, double-sided tape, and glassware, are excluded from the material usage and cost estimation.

5.2 Modeling Fabrication Time Differences

The fabrication time for creating a circuit on a new substrate is the sum of trace engraving time, determined by the path length (L_t), and board outline cutting time. The feed rate (F_t) depends on the engraving bit. The number of passes is determined by the ceiling of the fraction of the engraving depth (d_t)—typically 0.15 mm—and the stepdown (δz_t), which also depends on the engraving bit. The board outline engraving time is calculated in the similar manner, based on the outline length (L_o), feed rate (F_o), board thickness as cutting depth (d_o), and stepdown (δz_o). The total fabrication time can be estimated as follows:

$$T_{FR-4} = \frac{L_t}{F_t}\lceil\frac{d_t}{\delta z_t}\rceil + \frac{L_o}{F_o}\lceil\frac{d_o}{\delta z_o}\rceil$$

The fabrication time in PCB Renewal comprises several components: desoldering time, solder pad cleaning time, epoxy deposition time, epoxy curing time, engraving time, and an optional laser cutting time for manufacturing the deposition stencil. Desoldering time and solder pad cleaning time are highly dependent on the equipment used and the operator's skill level. In practice, desoldering time (T_{de}) requires user estimation based on their specific scenario. The default value for desoldering time is set to 1 minute, as all example circuits in our experiments were desoldered within this time frame using a hot plate. The solder pad cleaning time (T_{cl}) is calculated as the number of solder pads on the old board (n_p) multiplied by the estimated cleaning time per pad (t_p). Based on empirical experiments, the typical cleaning time per solder pad using a soldering iron is approximately 6 seconds. This value is set as the default, but users can adjust it to match their skill level. Epoxy is deposited along the contours of the conductors designated for removal, with the extruder moving at a constant rate during deposition. The estimated deposition time (T_d) is calculated based on the total deposition path length (L_d) and the feed rate (F_d), which is set at 3 mm/s for manual deposition.

$$T_d = \frac{L_d}{F_d}$$

Epoxy curing time (T_c) is a fixed duration specified in the conductive epoxy's datasheet. Engraving time consists of the same two components as engraving a new board: trace engraving time and board outline cutting time. These are calculated using the methods described above, with the corresponding path lengths denoted as L'_t for trace engraving and L'_o for board outline modification cutting. The primary difference lies in the trace engraving depth. In PCB Renewal, the new conductors must be engraved 0.05 mm deeper than previous iterations (see Section 4.4). Since the current renewal

is the n^{th} iteration, the engraving depth is:

$$d'_t = d_t + 0.05(n-1)$$

The stencil cutting time is estimated based on the contour length of the conductors to be removed (L_s) and the feed rate of a CO_2 laser cutter (F_l). Hence, the time difference between renewing and engraving a new PCB is:

$$T_{delta} = T_{de} + n_p t_p + \frac{L_d}{F_d} + T_c + \frac{L_s}{F_l} + \frac{L'_t}{F_t}\lceil\frac{d'_t}{\delta z_t}\rceil - \frac{L_t}{F_t}\lceil\frac{d_t}{\delta z_t}\rceil + \frac{L'_o - L_o}{F_o}\lceil\frac{d_o}{\delta z_o}\rceil$$

5.3 Modeling Energy Consumption Differences

The primary energy consumption arises from the epoxy heat curing process, as well as the power drawn by machinery for epoxy deposition, engraving, and stencil fabrication. Energy consumption for desoldering, pad cleaning, deposition, engraving and stencil cutting is calculated by multiplying the estimated time for each stage by its respective power consumption. Thus, the difference in energy consumption can be expressed as:

$$E_{delta} = T_{de}P_{de} + n_p t_p P_i + \frac{L_d}{F_d}P_d + T_c P_c + \frac{L_s}{F_l}P_l + (\frac{L'_t}{F_t}\lceil\frac{d'_t}{\delta z_t}\rceil - \frac{L_t}{F_t}\lceil\frac{d_t}{\delta z_t}\rceil + \frac{L'_o - L_o}{F_o}\lceil\frac{d_o}{\delta z_o}\rceil)P_e$$

where, P_i denotes the power required by the soldering iron.

6 Software

The PCB Renewal software (open-sourced on GitHub[1]) serves three main purposes: visualizing and enabling direct comparison of two circuit designs, generating stencil profiles for epoxy filling and milling profiles for selective trace renewal, and automatically estimating the material usage, cost, time, and energy consumption savings or trade-offs of a given design. The software is developed as a plug-in for the open-source EDA software KiCAD. The plug-in uses KiCAD's Python bindings[2] to access PCB data, shapely[3] for geometric operations, and wxPython[4] for the user interface.

6.1 Software Plug-in Features

The user interface includes a sequence of essential features: loading EDA files, aligning design layouts, selecting PCB layers for comparison, executing the comparison process, conducting sustainability analyses, and exporting cutting profiles. A responsive visualization panel remains active throughout the workflow, providing real-time updates based on user interactions to ensure immediate feedback.

Board Comparison. Our software allows users to load two KiCad PCB designs for comparison (Figure 10a). Because the designs may vary in size and position, an optional feature enables users to align them using selected reference points, such as the corners of board outline bounding boxes or the geometric centers of electronic component footprints (Figure 10b). Once aligned, the software executes the comparison algorithm in the background and displays the results in the visualization window.

[1]Software plug-in: https://github.com/zyyan20h/PCBRenewal.git
[2]KiCAD Python Bindings: https://dev-docs.kicad.org/en/apis-and-binding/pcbnew/
[3]shapely: https://shapely.readthedocs.io/en/stable/
[4]wxPython: https://wxpython.org/index.html

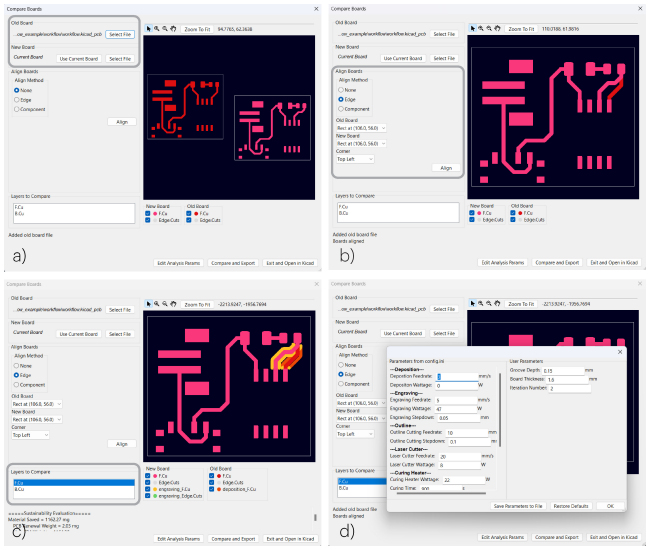

Figure 10: User Interface: a) importing boards, b) board alignment, c) board comparison, d) sustainability analysis parameters made customizable for different machine and tooling adoption.

Output and Analysis. After comparison, the software automatically exports the stencil profile and engraving pattern as fabrication inputs to the same directory as the "new board" design. While exporting these files, the software also performs a sustainability analysis for the given renewal scenario and displays the result in the log at the bottom of the plug-in interface. Based on these results, users can decide whether to proceed with PCB Renewal or create a new PCB from scratch. Calculation parameters are initialized with default values that match the machines and tools used in our demonstrations. Users can reconfigure these parameters in a pop-up window by clicking the "Edit Analysis Params" button (Figure 10d).

6.2 PCB Design Comparison Algorithms

The circuit design comparison results are used as both fabrication input and sustainability impact analysis data. This process requires highly accurate output to ensure minimal fabrication errors and reliable analysis results. To achieve a precise comparison between two KiCad board designs, we developed a custom algorithm that extracts board information from KiCad and converts it into vector-based geometries.

We used KiCAD's Python bindings to access the board information. Every PCB component (e.g. pads, tracks, holes) incorporated in our comparison algorithm is represented as a user-defined instance to preserve the integrity of the original data. Each board is represented by an instance of a custom `Board` class. A `Board` instance contains a collection of nets—groups of electrical nodes (or pins) and tracks that are electrically connected on copper layers. These nets are stored in a nested hash map, H, where each key corresponds to a layer names (e.g., `F.Cu` for the front layer or `B.Cu` for the back layer), and each key points to a list of nets present on that

layer. Nets are represented by a custom class, and each net instance contains a list of tracks, a list of pads, and the layer name to which it belongs. When the boards are imported, we initialize the board instances according to the layer and net information retrieved from KiCad. We refer to the two board instances as B_{old} and B_{new}, and their respective net hash maps as H_{old} and H_{new}.

The comparison is carried out in two steps. First, all nets from the old board are compared against each net of the new board. This step identifies nets with identical geometry and position, which remain unchanged and can be excluded from further comparison.

Next, the remaining nets in both board instances are converted into flat polygons and subjected to Boolean union operations within each board. A second round of comparison is then performed on the resulting compound polygon outlines, producing the final comparison results.

Net Wise Comparison. This step takes H_{old} and H_{new}, and generates two new hash maps, H_{old_unique} and H_{new_unique}, each containing nets with unique geometries from their respective boards.[5] If the two boards share no common nets, then H_{old_unique} will contain all the net instances from B_{old} and H_{new_unique} will contain all the conductors from B_{new}. The pseudocode block below illustrates the pairwise comparison of each list of nets within the corresponding layers of the boards.

Algorithm 1: compareNets(H_{old}, H_{new}, S)

in: Hash map of nets on the old board H_{old}, Hash map of nets on the new board H_{new}, Layers selected for comparison S
out: Hash map of unique old nets H_{old_unique}, Hash map of unique new nets H_{new_unique}
local: Flag denoting whether a net in the old board has an identical match in the new board F

(1) $H_{old\_unique} \leftarrow$ empty hash map
(2) $H_{new\_unique} \leftarrow$ empty hash map
(3) **for each** layer L in S **do**:
(4) $\quad H_{old\_unique}[L] \leftarrow$ empty list
(5) $\quad H_{new\_unique}[L] \leftarrow H_{new}[L]$
(6) $\quad$ **for each** old net N_{old} in $H_{old}[L]$ **do**:
(7) $\quad\quad F \leftarrow$ FALSE
(8) $\quad\quad$ **for each** new net N_{new} in $H_{new\_unique}[L]$ **do**:
(9) $\quad\quad\quad$ **if** $N_{old} = N_{new}$ **then:**
(10) $\quad\quad\quad\quad F \leftarrow$ TRUE
(11) $\quad\quad\quad\quad$ **Pop** N_{new} from $H_{new\_unique}[L]$
(12) $\quad\quad\quad\quad$ **Exit loop**
(13) $\quad\quad$ **if not** F **then**:
(14) $\quad\quad\quad$ **Append** N_{old} to $H_{old\_unique}[L]$
(15) **Return** H_{old_unique}, H_{new_unique}

When comparing two nets (line 9 in Algorithm 1), we verify that the position and geometry of all pads and tracks in both nets are identical.

[5]We use the notation hashmap[key] ← value to represent inserting or updating a value associated with a specific key in the hash map, mirroring Python's dictionary syntax.

Geometric Comparison. In this step, we convert all remaining unique nets into polygons for further comparison. Algorithm 2 details the parsing process for these remaining nets within a single board.

Algorithm 2: createPaths(H, S)

in: Hash map of nets H, Layers to compare
out: Hash map of paths P
local: offset outline of an individual net p_{net}, compound geometry of all net in a layer p

(1) $P \leftarrow$ empty hash map
(2) **for each** layer L in S **do**:
(3) $\quad p \leftarrow$ blank shape
`// place holder for the Boolean union paths`
(4) $\quad$ **for each** net N in $H[L]$ **do**:
(5) $\quad\quad p_{net} \leftarrow$ offset outline of N
(6) $\quad\quad p \leftarrow$ **Boolean union** of p and p_{net}
(7) $\quad P[L] \leftarrow p$
(8) **Return** P

For each net—whether it is to be removed from the old board design or engraved into the new one—the fabrication process focuses on the isolation area outside that net, either covering it or removing materials. The minimum width of the isolation area is usually defined in the design rule checking (DRC) configuration. To determine the midline of the isolation area, we offset the outlines of each net by half of the minimum isolation width. This midline conservatively represents any possible machining or deposition path outside the net. Within each board layer, we then compute the Boolean union of all polygons generated for the leftover nets in that layer, and store the resulting path in a new hash map P.

Using Algorithm 2, we parse the leftover nets across all layers in both boards. We then apply Boolean subtraction between the parsing results of each layer from each board (Algorithm 3). This process yields paths for deposition (D_{path}) and engraving (E_{path}), each having a equal to the minimum isolation width defined in DRC.

Algorithm 3: comparePaths(H_{old}, H_{new}, S)

in: Hash map of nets on the old board H_{old}, Hash map of nets on the new board H_{new}, Layers selected for comparison S
out: Hash map of paths to deposit D_{path}, Hash map of paths to engrave E_{path}

(1) $P_{old} \leftarrow$ createPaths(H_{old}, S)
(2) $P_{new} \leftarrow$ createPaths(H_{new}, S)
(3) $D_{path} \leftarrow$ empty hash map
(4) $E_{path} \leftarrow$ empty hash map
(5) **for each** layer L in S **do**:
(6) $\quad D_{path}[L] \leftarrow$ **Boolean subtraction** of $P_{old}[L]$ and $P_{new}[L]$
(7) $\quad E_{path}[L] \leftarrow$ **Boolean subtraction** of $P_{new}[L]$ and $P_{old}[L]$
(8) **Return** D_{path}, E_{path}

Note that, between individual renewal iterations, certain traces and pads from the old board do not need to be "erased" if the corresponding area is not utilized in the new board design. However, it is uncertain whether future iterations will make use of the areas these traces and pads occupy. To preserve the potential for all future renewal iterations, our software, by default, "erases" all undesired nets from the old board.

Support of Vias and Through-Hole Components. Vias are compared within their own category across the two boards. When a via from the old board is no longer used in the new design, it is replaced with a hole in the engraving profile. These holes, along with existing holes in the old board designed for through-hole components and mechanical assembly, are considered outside board usable profile and do not support new traces and pads. If any new traces or pads overlap with these areas, our software will generate an error message and a corresponding visualization layer in yellow color to alert the user.

Outline Comparison. In addition to comparing the copper layers, the plugin also compares the board outlines. It does this by by converting the board outlines into polygons and performing a Boolean subtraction on those polygons. This results in a polygon that serves as a guide for trimming the old board to convert it into the new one.

The plugin uses the shapely python library to perform geometric parsing and Boolean operations.

7 Example PCB Renewal Scenarios

In this section, we present a series of walkthrough examples. Sections 7.1 through 7.3 showcase a single CNC-milled substrate being reused across four design iterations within three distinct projects. Section 7.4 further demonstrates that PCB Renewal can be applied to factory-made, double-layer PCBs. These examples highlight how PCB Renewal facilitates local alterations to circuit traces and board outlines, enabling error correction and functional updates. Additionally, they demonstrate the versatility and range of electrical functionalities achievable with these updated hybrid material circuits.

We report the sustainability analysis results for each example. For trace engraving, we used a 1/64-inch square end mill, while a 1/32-inch square end mill was used for outline engraving. The corresponding tooling parameters were applied to estimate the fabrication time. Additionally, we measured the average power consumption of our machines using an appliance wattage monitor. During operation, the CNC machine consumes approximately 47 W for engraving, the hotplate averages 22 W for desoldering, the solder iron used for pad cleaning consumes 21.5 W, the laser cutter requires 8 W for stencil cutting, and the heater operates at an average of 22 W during the heat-curing process. We set the desoldering time to 1 minute and the cleaning time for each solder pad to 3 seconds. These values are used as inputs for energy estimation. The standardized analysis data are visualized in radar graphs for each renewal iteration.

7.1 Iteration One and Two — Camera Roller

In this example, we created a camera roller designed to achieve fluid, dynamic shots, such as tracking, panning, and dollying. The original circuit board was developed to control two DC gear motors using an ESP8266 microcontroller. However, an error was identified in the ESP8266 accessory circuit—its enable pin requires an external pull-up resistor when resetting the board or entering download mode, preventing us from uploading code to the ESP8266.

To correct this, we needed to add a resistor and connect it to two existing conductors, which also required relocating some components and traces. In a conventional PCB prototyping process, this would have required manufacturing an entirely new PCB, as traces cannot be easily altered or added.

With PCB Renewal, however, we were able to make these minor adjustments directly on the existing prototype. This enabled us to implement the necessary modifications without the waste of materials or energy required to fabricate a new board. The corrected PCB now functions as intended, allowing control code to be uploaded and ensuring smooth operation of the camera roller (see the left column of Figure 11).

Between the first and second design iterations, PCB Renewal allowed us to save 6402.90 mg of FR-4, 71.91 kJ of energy and 15.25 min in fabrication time, while consuming only 4.06 mg of silver epoxy, reducing the cost of raw material by 98.4%.

7.2 Iteration Three — WiFi Radio

With the camera roller design finalized, the prototype PCB was no longer needed. However, much of its circuitry, especially the sections supporting the ESP8266 microcontroller, remained potentially useful for other projects. Instead of discarding the entire board, we selectively removed and updated only the necessary components of the camera roller PCB, repurposing it for a new project.

In this case, we transformed the otherwise obsolete camera roller PCB into a WiFi radio controller while retaining much of the original microcontroller circuitry. The modifications mainly involved swapping out the motor driver and connectors for an audio amplifier, speaker connections, and a potentiometer. We designed the new circuit layout using KiCAD and utilized the PCB Renewal plug-in to evaluate the sustainable impact of updating the old board. We then physically implemented the updated PCB by selectively removing and updating the traces and pads, as well as reducing the board size to fit the new radio design. The renewal process is documented in the middle column of Figure 11.

In addition to demonstrating how PCB Renewal can support the prototyping of a complete new project using an obsolete PCB, this WiFi radio example also showed that the renewed PCB, with circuit traces made from hybrid materials, could support audible-frequency data transmission while maintaining low noise levels.

In this design iteration, renewing the PCB allowed us to save 5602.15 mg of FR-4 and 32.03 kJ of energy while consuming only 105 mg of silver epoxy, reducing material cost by 74.6%. The fabrication time is comparable to engraving a new piece of FR-4, with PCB Renewal taking only 3.89 minutes longer despite the additional desoldering and cleaning steps.

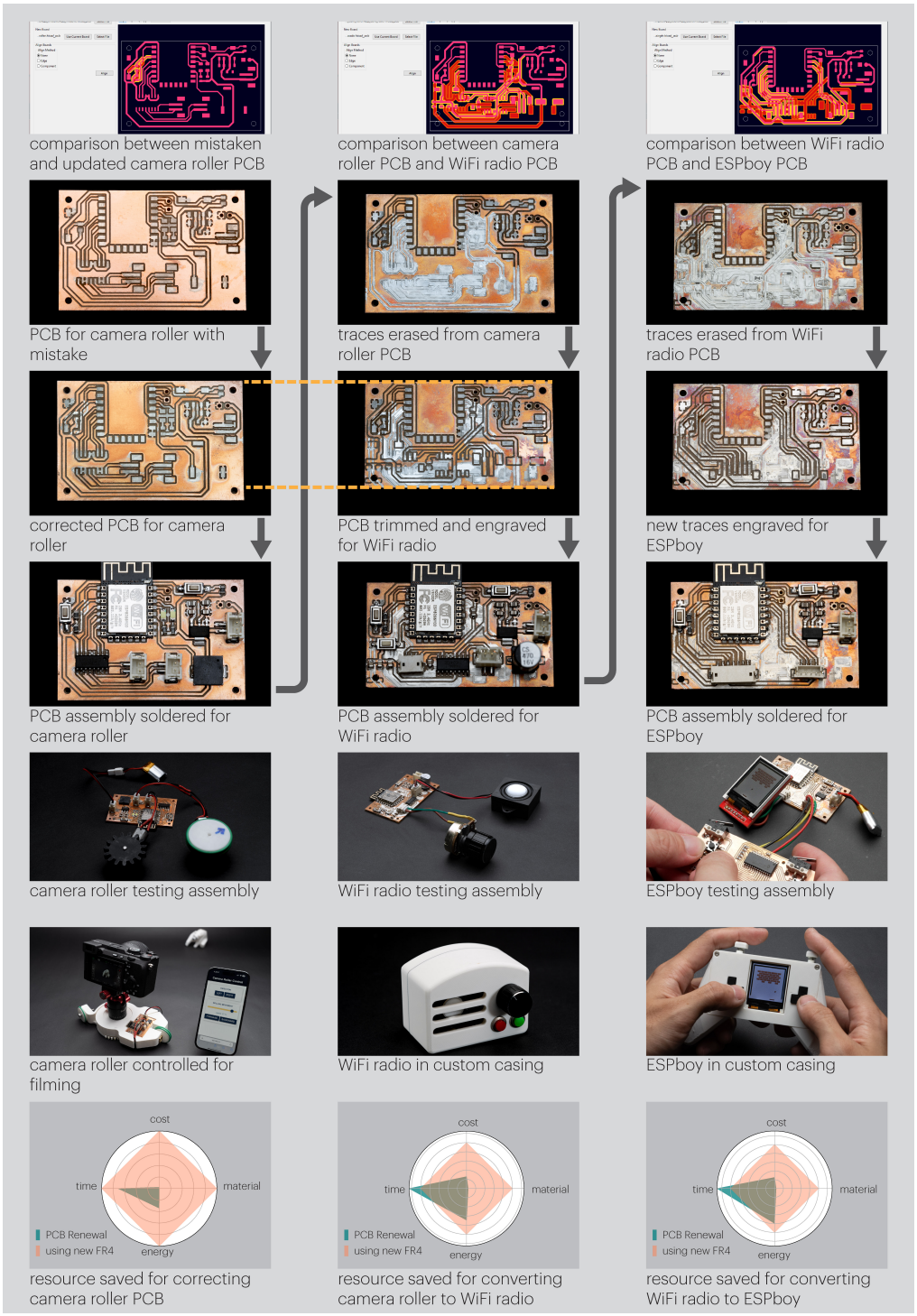

Figure 11: Multi-iteration renewal on a single piece of FR-4. Each column presents the software-generated PCB comparison result, the renewal process, the prototype assembly, and the amount of resources saved. Left column: correction of a mistaken connection in the camera roller PCB. Middle column: trimming the board size and modifying part of the camera roller circuit for the WiFi radio prototype. Right column: converting the WiFi radio circuit into the ESPboy motherboard, along with a daughterboard to expand functionality.

7.3 Iteration Four — ESPBoy Game Console

One FR-4 board can undergo multiple iterations across different projects. Here, we demonstrate that the same PCB substrate can be reused for yet another new project, even after three prior iterations.

Specifically, we retrofitted the previous WiFi radio controller into a game console based on the open-source ESPBoy design [23]. In this iteration, we repurposed the WiFi radio circuit as the motherboard of the ESPBoy assembly, retaining the ESP8266 circuitry and adding two multi-pin JST connectors. Additionally, we fabricated a daughterboard that hosts an OLED display and joystick controls, serving as the console's main input and output interface. These components were positioned ergonomically to ensure comfortable operation. The multi-pin JST connectors linked the ESP8266 motherboard with the daughterboard.

The updated motherboard effectively handled high-frequency, real-time data transmission, as demonstrated by the I²C communication at 100 kbit/s between the microcontroller, the display, and the GPIO extender that processed the button inputs. The renewal process is documented in the right column of Figure 11.

While this iteration introduced an additional PCB, we still reduced material waste by largely reusing the original PCB as the motherboard of the ESPBoy game console. Specifically, we saved 5608.24 mg of FR-4 and 25.99 kJ of energy while consuming only 98.91 mg of silver epoxy, reducing material costs by 87.5%. The fabrication time remains comparable to engraving a new FR-4 board, with a difference of less than 5 min.

7.4 Renewing an Outsourced PCB

While previous examples showcased how PCB Renewal reduces material waste for CNC-milled PCBs, its versatility extends to factory-made PCBs, such as those ordered online or found in commercial electronic devices. In this example, we repurposed a digital LED watch PCB, manufactured as a double-layer board with a solder mask by a small-batch PCB producer, into a PCB for an interactive cat toy.

We began by outsourcing an open-source LED watch PCB [49] to a small-batch manufacturer. The PCB featured a standard double-layer configuration, a black solder mask, and a round shape (top image in the left column of Figure 12). Since the manufacturer requires a minimum order quantity of five PCBs, we had several extra boards remaining after successfully assembling the LED watch (shown in the bottom images of the left column in Figure 12). Typically, such boards are difficult to reuse in other projects due to their specific design. However, with the PCB Renewal approach, these surplus PCBs can be easily repurposed. In this case, they were modified to function as the controller for an interactive cat toy ball.

The renewal process for an outsourced, double-sided PCB is largely identical to that of an in-house, CNC-milled PCB, with two exceptions: the removal of the solder mask in the area to be modified, and the editing of vias, if necessary.

Removing the solder mask was based on the engraving profile generated from the KiCAD plug-in (top image in the right column of Figure 12). Specifically, the plug-in computed the areas of difference between the original LED watch PCB and the newly designed toy PCB for both sides. These differential areas were then sent to a CO_2 laser cutter, which selectively removed the solder mask and exposed the copper conductors using rastering mode (row two in the right column of Figure 12). Alternatively, the solder mask can be removed using either a 1064 nm wavelength fiber laser [69] or a diode laser [53].

In the new toy ball circuit design, new trace areas required electrical connections between both sides of the PCB, while some existing vias from the original PCB needed to be removed. To achieve this, undesired vias were drilled out using a square end mill during the

Figure 12: Renewal of an outsourced double-layer PCB: the left column shows the production of LED watch PCBs, including assembly into a working watch. The right column illustrates the renewal process, showcasing PCB design comparisons, solder mask removal, and board modifications for a cat toy, and its final assembly. A radar chart highlights the resources saved through PCB Renewal versus creating a new FR4 board.

engraving process. New vias are created using the same process, followed by either manual soldering into these through-holes to establish electrical connections or filling the entire via hole with conductive epoxy. The modified PCB is shown in row three of the right column in Figure 12.

The repurosed PCB was then assembled and installed into a custom 3D printed housing to complete the final cat toy (row four in the right column of Figure 12). The renewal process significantly reduced material waste, manufacturing energy, and fabrication time. The sustainability modeling results are presented at the bottom of right column in Figure 12. These estimates assume that the benchmark board is made using a CNC FR-4 board and account for the energy required for laser cutting during solder mask removal.

PCB Renewal notably provides a much shorter turnaround time compared to ordering new PCBs from a manufacturer. Furthermore, it eliminates shipping-related energy costs, making PCB Renewal a more efficient and sustainable solution.

8 Discussion

PCB Renewal enables multiple iterations on a single FR-4 substrate, both within and across projects, promoting more sustainable PCB making practices. However, this approach also has its limitations. In this section, we discuss these limitations and outline potential future research opportunities.

8.1 Unpacking Sustainability Benefits and Trade-Offs

Across various examples and design iterations, we observed consistent savings in materials, costs, and energy, though time savings varied. For example, in the iteration of the camera roller for the same project, PCB Renewal saved up to 60% of the time by re-engraving only a small section of copper rather than engraving all traces on a fresh substrate. In other cases, such as the ESPboy, PCB Renewal required slightly more time than fabricating a new PCB due to the increased amount of editing required. From the timing perspective, if a circuit design is straightforward to mill, the renewal approach might not be time-efficient. This underscores that the decision between creating a PCB from scratch and using PCB Renewal is case-dependent and dynamic. The sustainability model developed in Section 5, along with its implementation in the software plug-in (Section 6), provides end-users a practical tool for making informed decisions by offering comprehensive comparison data for each design iteration.

However, our current sustainability model has its own limitations and can be further improved. For example, the time and energy costs associated with the delivery of outsourced PCBs are not currently factored in, even though delivery is often the most time-consuming aspect of the PCB manufacturing process. In fact, if delivery time is considered, renewing a factory-made PCB is almost always more time-efficient than ordering a new one.

Additionally, the current calculation of material savings is rudimentary, focusing solely on the total weight of the material involved. Ideally, the model would be more precise and informative if it considered the carbon footprint of the FR-4 material saved in comparison to the additional use of silver-epoxy. However, since carbon footprint data for silver-epoxy is unavailable, total weight remains one of the few standardized metrics accessible for comparing different materials. This limitation highlights the need for a more open-data approach to LCA [19, 47], particularly as new materials are developed and introduced to the market.

8.2 Automating PCB Renewal

While our current work has evaluated PCB Renewal in terms of material, time, and energy costs, other practical factors must be considered, such as the increased likelihood of manual errors introduced during the renewal process. For example, manually depositing silver-epoxy may require skills and experience, while curing the epoxy-filled PCB necessitates transferring the board to an additional heating device. Additionally, cutting new traces on an existing board needs precise alignment, requiring users to carefully position the board in the CNC machine. For some users, these extra steps and the increased risk of manual mistakes are important trade-offs to consider when weighing PCB Renewal against the simplicity of creating a new board from scratch.

We envision that a few simple upgrades to a desktop CNC machine could reduce some of the labor effort, making PCB Renewal more accessible. For example, epoxy deposition could be automated with desktop CNC machines that support syringe extruders. In addition, the CNC cutting plate could be equipped with a heating element (e.g., a 3D printer heating bed), allowing the curing process to be integrated into the automated workflow within the CNC machine. Finally, alignment could also be automated, for example, through a camera-based calibration process. If these changes are implemented, we can potentially transform an off-the-shelf CNC machine designed for making PCBs into one that also supports the remaking or renewal process, promoting more sustainable PCB making practices.

8.3 Supported PCB Materials and Types

This paper focuses on the FR-4 PCB substrate, as it is the most commonly used material for both in-house and outsourced PCB production. However, other more environmentally friendly PCB substrates, such as paper-based FR-1 or cellulose-based FR-3, might also be compatible with the current workflow, though we have not explored these options. We suspect that working with FR-1 or FR-3 materials may require alternative conductive epoxies that cure through UV processes rather than heat, given these substrates' lower operating temperature. This suggests a potential future direction for comprehensively understanding the comparability of different substrate materials and conductive epoxies.

Our method supports single- and double-layer PCBs, whether manufactured in-house or outsourced. While our example (Section 7.4) demonstrates the technical viability of renewing and updating externally manufactured PCBs, it depends on having access to the original circuit design. For commercial PCBs that are not open source, this requirement poses a significant obstacle. To enable the renewal process for commercial PCBs, reverse engineering techniques utilizing X-ray tomography [3, 10] or computer vision [44] would be necessary. However, integrating this approach into the current workflow remains an open question and requires further research.

8.4 Toward PCB Reuse in the Long Run

Our work primarily explores the technical feasibility of PCB Renewal. However, achieving a long-term impact in sustainable making requires understanding end-users' willingness to adopt PCB Renewal, which necessitates deployment and active community engagement.

As a first step, we have open-sourced the PCB Renewal software plug-in (Section 6). Future deployment will allow us to explore integrating PCB Renewal with other complementary methods that support PCB reuse. For example, the SolderlessPCB [68] method enables the reuse of electronic components without soldering, while ecoEDA [42] facilitates component reuse across multiple projects. It would be interesting to explore whether a more integrated and comprehensive PCB reuse system could influence end-users' PCB making and usage practice over time.

Finally, while this paper primarily considers PCB Renewal in the context of individual PCB fabrication, it also holds potential for industrial-scale recycling. For example, integrating a PCB layout recognition system into recycling facilities could potentially enable centralized operations to adopt PCB Renewal, allowing useful PCBs to be repurposed before entering the waste stream. Investigating industrial applications could uncover new opportunities for PCB Renewal on a larger scale.

9 Conclusion

In this paper, we introduced PCB Renewal, a novel technique that "erases" and "reconfigures" existing circuit traces. We presented PCB Renewal workflow and evaluate its electrical performance and mechanical durability. We modeled the sustainability impact of PCB Renewal by calculating the material usage, cost, power, and time consumption for renewing PCB versus using new substrates. We implemented a custom EDA software plug-in that guides epoxy deposition, generates updated profiles, and calculates resource use. We showcased the effectiveness of PCB Renewal with a set of walkthrough examples, and concluded the paper by discussing its limitations and proposing future directions.

Acknowledgments

We thank Sandbox, the Jagdeep Singh Family Makerspace, for providing access to tools during the development and documentation of this project. We also thank our cat, Zhu Yuanzhang, for enjoying the custom cat toy and serving as a great model for Figure 12. An LLM service was used exclusively for proofreading.

References

[1] Altium. 2024. Altium. https://support.bantamtools.com/hc/en-us/articles/115001656813-Altium. Accessed: 09-11-2024.

[2] Vicente Arroyos, Maria L K Viitaniemi, Nicholas Keehn, Vaidehi Oruganti, Winston Saunders, Karin Strauss, Vikram Iyer, and Bichlien H Nguyen. 2022. A Tale of Two Mice: Sustainable Electronics Design and Prototyping. In *Extended Abstracts of the 2022 CHI Conference on Human Factors in Computing Systems* (New Orleans, LA, USA) *(CHI EA '22)*. Association for Computing Machinery, New York, NY, USA, Article 263, 10 pages. https://doi.org/10.1145/3491101.3519823

[3] Navid Asadizanjani, Mark Tehranipoor, and Domenic Forte. 2017. PCB Reverse Engineering Using Nondestructive X-ray Tomography and Advanced Image Processing. *IEEE Transactions on Components, Packaging and Manufacturing Technology* 7, 2 (2017), 292–299. https://doi.org/10.1109/TCPMT.2016.2642824

[4] Cornelis P. Baldé, Ruediger Kuehr, Tales Yamamoto, Rosie McDonald, Elena D'Angelo, Shahana Althaf, Garam Bel, Otmar Deubzer, Elena Fernandez-Cubillo, Vanessa Forti, Vanessa Gray, Sunil Herat, Shunichi Honda, Giulia Iattoni, Deepali S. Khetriwal, Vittoria Luda di Cortemiglia, Yuliya Lobuntsova, Innocent Nnorom, Noémie Pralat, and Michelle Wagner. 2024. The Global E-waste Monitor 2024. *International Telecommunication Union (ITU) and United Nations Institute for Training and Research* (2024). ISBN pdf: 978-92-61-38781-5.

[5] Bantam. 2024. Othermill (V2). https://support.bantamtools.com/hc/en-us/articles/115001668853-Othermill-V2. Accessed: 09-11-2024.

[6] Fiona Bell, Latifa Al Naimi, Ella McQuaid, and Mirela Alistar. 2022. Designing with Alganyl. In *Sixteenth International Conference on Tangible, Embedded, and Embodied Interaction* (Daejeon, Republic of Korea) *(TEI '22)*. Association for Computing Machinery, New York, NY, USA, Article 2, 14 pages. https://doi.org/10.1145/3490149.3501308

[7] Fiona Bell, Derrek Chow, Hyelin Choi, and Mirela Alistar. 2023. SCOBY BREASTPLATE: SLOWLY GROWING A MICROBIAL INTERFACE. In *Proceedings of the Seventeenth International Conference on Tangible, Embedded, and Embodied Interaction* (Warsaw, Poland) *(TEI '23)*. Association for Computing Machinery, New York, NY, USA, Article 34, 15 pages. https://doi.org/10.1145/3569009.3572805

[8] Kurki N. Bharath, Puttegowda Madhu, Thyavihalli G. Y. Gowda, Akarsh Verma, Mavinkere R. Sanjay, and Suchart Siengchin. 2020. A novel approach for development of printed circuit board from biofiber based composites. *Polymer Composites* 41, 11 (2020), 4550–4558. https://doi.org/10.1002/pc.25732

[9] Eli Blevis. 2007. Sustainable Interaction Design: Invention & Disposal, Renewal & Reuse. In *Proceedings of the SIGCHI Conference on Human Factors in Computing Systems* (San Jose, California, USA) *(CHI '07)*. Association for Computing Machinery, New York, NY, USA, 503–512. https://doi.org/10.1145/1240624.1240705

[10] Ulbert J Botero, David Koblah, Daniel E Capecci, Fatemeh Ganji, Navid Asadizanjani, Damon L Woodard, and Domenic Forte. 2020. Automated via detection for PCB reverse engineering. In *International Symposium for Testing and Failure Analysis*, Vol. 83348. ASM International, 157–171. https://doi.org/10.31399/asm.cp.istfa2020p0157

[11] Leah Buechley, Ruby Ta, and Alyssa Johnson. 2023. 3D Printable Play-Dough. In *Extended Abstracts of the 2023 CHI Conference on Human Factors in Computing Systems (CHI EA '23)*. Association for Computing Machinery, New York, NY, USA, Article 428, 4 pages. https://doi.org/10.1145/3544549.3583927

[12] MG Chamicals. 2024. Technical data sheet of 4902P. https://mgchemicals.com/downloads/tds/tds-4902p.pdf. Accessed: 09-11-2024.

[13] Chemtronics. 2019. HOW-TO: PCB Trace Repair With Conductive Ink | Chemtronics. https://www.chemtronics.com/how-to-pcb-trace-repair-with-conductive-ink. Accessed: 09-11-2024.

[14] CJ Chen, JP Partridge, B Hussey, and A Gupta. 1991. Self-induced repair of printed circuit boards. *Plating and surface finishing* 78, 6 (1991), 45–49.

[15] Tingyu Cheng, Koya Narumi, Youngwook Do, Yang Zhang, Tung D. Ta, Takuya Sasatani, Eric Markvicka, Yoshihiro Kawahara, Lining Yao, Gregory D. Abowd, and HyunJoo Oh. 2020. Silver Tape: Inkjet-Printed Circuits Peeled-and-Transferred on Versatile Substrates. *Proc. ACM Interact. Mob. Wearable Ubiquitous Technol.* 4, 1, Article 6 (mar 2020), 17 pages. https://doi.org/10.1145/3381013

[16] Tingyu Cheng, Taylor Tabb, Jung Wook Park, Eric M Gallo, Aditi Maheshwari, Gregory D. Abowd, Hyunjoo Oh, and Andreea Danielescu. 2023. Functional Destruction: Utilizing Sustainable Materials' Physical Transiency for Electronics Applications. In *Proceedings of the 2023 CHI Conference on Human Factors in Computing Systems* (Hamburg, Germany) *(CHI '23)*. Association for Computing Machinery, New York, NY, USA, Article 366, 16 pages. https://doi.org/10.1145/3544548.3580811

[17] Tingyu Cheng, Zhihan Zhang, Han Huang, Yingting Gao, Wei Sun, Gregory D Abowd, HyunJoo Oh, and Josiah Hester. 2024. Recy-ctronics: Designing Fully Recyclable Electronics With Varied Form Factors. *arXiv preprint arXiv:2406.09611* (2024).

[18] Circuit Technology Center [n.d.]. 6.1 Jumper Wires. https://www.circuitrework.com/guides/6-1.html. Accessed: 09-11-2024.

[19] Andreas Cirotha, Claudia Di Noia, Salwa Syed Burhana, and Michael Srockaa. 2019. LCA database creation: Current challenges and the way forward. *Indonesian Journal of Life Cycle Assessment and Sustainability* 3, 2 (2019), 41–51.

[20] Himani Deshpande, Haruki Takahashi, and Jeeeun Kim. 2024. Unmake to Remake: Materiality-Driven Rapid Prototyping. *ACM Trans. Comput.-Hum. Interact.* 31, 6, Article 78 (Dec. 2024), 31 pages. https://doi.org/10.1145/3685270

[21] Kristin N. Dew and Daniela K. Rosner. 2019. Designing with Waste: A Situated Inquiry into the Material Excess of Making. In *Proceedings of the 2019 on Designing Interactive Systems Conference* (San Diego, CA, USA) *(DIS '19)*. Association for Computing Machinery, New York, NY, USA, 1307–1319. https://doi.org/10.1145/3322276.3322320

[22] Andrei Drumea and Cristina Ioana Marghescu. 2015. Analysis of current carrying capacity of silver-based conductive pastes for PCB repair. In *2015 IEEE 21st International Symposium for Design and Technology in Electronic Packaging (SIITME)*. 297–300. https://doi.org/10.1109/SIITME.2015.7342343

[23] ESPBoy: Open-source ESP8266 Game Console [n.d.]. https://www.espboy.com/. Accessed: 09-11-2024.

[24] Brian J Fogg. 2003. *Persuasive Technology: Using Computers to Change What We Think and Do*. Morgan Kaufmann, San Francisco, CA. https://doi.org/10.1016/B978-1-55860-643-2.X5000-8

[25] Jon Froehlich, Tawanna Dillahunt, Predrag Klasnja, Jennifer Mankoff, Sunny Consolvo, Beverly Harrison, and James A. Landay. 2009. UbiGreen: investigating a mobile tool for tracking and supporting green transportation habits. In *Proceedings of the SIGCHI Conference on Human Factors in Computing Systems* (Boston, MA, USA) *(CHI '09)*. Association for Computing Machinery, New York, NY, USA, 1043–1052. https://doi.org/10.1145/1518701.1518861

[26] Daniel Groeger and Jürgen Steimle. 2018. ObjectSkin: Augmenting Everyday Objects with Hydroprinted Touch Sensors and Displays. *Proc. ACM Interact. Mob. Wearable Ubiquitous Technol.* 1, 4, Article 134 (jan 2018), 23 pages. https://doi.org/10.1145/3161165

[27] Sofia Guridi, Emmi Pouta, Ari Hokkanen, and Aayush Jaiswal. 2023. LIGHT TISSUE: Development of Cellulose-Based Optical Textile Sensors. In *Proceedings of the Seventeenth International Conference on Tangible, Embedded, and Embodied Interaction* (Warsaw, Poland) *(TEI '23)*. Association for Computing Machinery, New York, NY, USA, Article 27, 14 pages. https://doi.org/10.1145/3569009.3572798

[28] Michael Z Hauschild, Ralph K Rosenbaum, Stig Irving Olsen, et al. 2018. *Life Cycle Assessment: Theory and Practice*. Springer International Publishing, Cham, Switzerland. https://doi.org/10.1007/978-3-319-56475-3

[29] Emily Hsu, Katayun Barmak, Alan C. West, and Ah-Hyung A. Park. 2019. Advancements in the treatment and processing of electronic waste with sustainability: a review of metal extraction and recovery technologies. *Green Chem.* 21 (2019), 919–936. Issue 5. https://doi.org/10.1039/C8GC03688H

[30] Xian Huang, Yuhao Liu, Suk-Won Hwang, Seung-Kyun Kang, Dwipayan Patnaik, Jonathan Fajardo Cortes, and John A. Rogers. 2014. Biodegradable Materials for Multilayer Transient Printed Circuit Boards. *Advanced Materials* 26, 43 (2014), 7371–7377. https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.201403164

[31] Nathaniel Hudson, Celena Alcock, and Parmit K. Chilana. 2016. Understanding Newcomers to 3D Printing: Motivations, Workflows, and Barriers of Casual Makers. In *Proceedings of the 2016 CHI Conference on Human Factors in Computing Systems* (San Jose, California, USA) *(CHI '16)*. Association for Computing Machinery, New York, NY, USA, 384–396. https://doi.org/10.1145/2858036.2858266

[32] Giles Humpston and David M. Jacobson. 2004. *Principles of Soldering*. ASM International. https://doi.org/10.31399/asm.tb.ps.9781627083522

[33] Ayaka Ishii, Kunihiro Kato, Kaori Ikematsu, Yoshihiro Kawahara, and Itiro Siio. 2021. Fabricating Wooden Circuit Boards by Laser Beam Machining. In *Adjunct Proceedings of the 34th Annual ACM Symposium on User Interface Software and Technology* (Virtual Event, USA) *(UIST '21 Adjunct)*. Association for Computing Machinery, New York, NY, USA, 109–111. https://doi.org/10.1145/3474349.3480191

[34] Elvin Karana, Davine Blauwhoff, Erik-Jan Hultink, and Serena Camere. 2018. When the Material Grows: A Case Study on Designing (with) Mycelium-Based Materials. *International Journal of Design* 12, 2 (2018), 119–136. http://www.ijdesign.org/index.php/IJDesign/article/view/2918

[35] Yoshihiro Kawahara, Steve Hodges, Benjamin S. Cook, Cheng Zhang, and Gregory D. Abowd. 2013. Instant Inkjet Circuits: Lab-Based Inkjet Printing to Support Rapid Prototyping of UbiComp Devices. In *Proceedings of the 2013 ACM International Joint Conference on Pervasive and Ubiquitous Computing* (Zurich, Switzerland) *(UbiComp '13)*. Association for Computing Machinery, New York, NY, USA, 363–372. https://doi.org/10.1145/2493432.2493486

[36] Sunyoung Kim and Eric Paulos. 2011. Practices in the Creative Reuse of E-Waste. In *Proceedings of the SIGCHI Conference on Human Factors in Computing Systems* (Vancouver, BC, Canada) *(CHI '11)*. Association for Computing Machinery, New York, NY, USA, 2395–2404. https://doi.org/10.1145/1978942.1979292

[37] Marion Koelle, Madalina Nicolae, Aditya Shekhar Nittala, Marc Teyssier, and Jürgen Steimle. 2022. Prototyping Soft Devices with Interactive Bioplastics. In *Proceedings of the 35th Annual ACM Symposium on User Interface Software and Technology* (Bend, OR, USA) *(UIST '22)*. Association for Computing Machinery, New York, NY, USA, Article 19, 16 pages. https://doi.org/10.1145/3526113.3545623

[38] Mannu Lambrichts, Raf Ramakers, Steve Hodges, James Devine, Lorraine Underwood, and Joe Finney. 2023. CircuitGlue: A Software Configurable Converter for Interconnecting Multiple Heterogeneous Electronic Components. *Proc. ACM Interact. Mob. Wearable Ubiquitous Technol.* 7, 2, Article 63 (June 2023), 30 pages. https://doi.org/10.1145/3596265

[39] Bernd Lange. 2005. PCB machining and repair via laser. *OnBoard Technol* 2, 1 (2005), 12–14.

[40] Eldy S. Lazaro Vasquez, Mirela Alistar, Laura Devendorf, and Michael L. Rivera. 2024. Desktop Biofibers Spinning: An Open-Source Machine for Exploring Biobased Fibers and Their Application Towards Sustainable Smart Textile Design. In *Proceedings of the CHI Conference on Human Factors in Computing Systems* (Honolulu, HI, USA) *(CHI '24)*. Association for Computing Machinery, New York, NY, USA, Article 856, 18 pages. https://doi.org/10.1145/3613904.3642387

[41] Chin Huat Joel Lim, C. S. Suchand Sandeep, Vadakke Matham Murukeshan, and Young-Jin Kim. 2021. Direct Laser Writing of Graphene-Based Electrical Interconnects for Printed Circuit Board Repair. *Advanced Materials Technologies* 6, 12 (2021), 2100514. https://doi.org/10.1002/admt.202100514

[42] Jasmine Lu, Beza Desta, K. D. Wu, Romain Nith, Joyce E Passananti, and Pedro Lopes. 2023. EcoEDA: Recycling E-Waste During Electronics Design. In *Proceedings of the 36th Annual ACM Symposium on User Interface Software and Technology* (San Francisco, CA, USA) *(UIST '23)*. Association for Computing Machinery, New York, NY, USA, Article 30, 14 pages. https://doi.org/10.1145/3586183.3606745

[43] Jasmine Lu and Pedro Lopes. 2024. Re-Envisioning the Role of a User in Sustainable Computing. *IEEE Pervasive Computing* 23, 2 (2024), 38–44. https://doi.org/10.1109/MPRV.2024.3383793

[44] Jasmine Lu, Sai Rishitha Boddu, and Pedro Lopes. 2025. ProtoPCB: Reclaiming Printed Circuit Board E-waste as Prototyping Material *(CHI '25)*. Association for Computing Machinery, New York, NY, USA. https://doi.org/10.1145/3613904.3642765

[45] Leah Maestri and Ron Wakkary. 2011. Understanding repair as a creative process of everyday design. In *Proceedings of the 8th ACM Conference on Creativity and Cognition* (Atlanta, Georgia, USA) *(C&C '11)*. Association for Computing Machinery, New York, NY, USA, 81–90. https://doi.org/10.1145/2069618.2069633

[46] Cristina I. Marghescu, Andrei Drumea, and Bogdan T. Mihailescu. 2015. Investigation on current capabilities of Ni-based conductive pastes for PCB repair. In *2015 38th International Spring Seminar on Electronics Technology (ISSE)*. 324–328. https://doi.org/10.1109/ISSE.2015.7248015

[47] A. Martínez-Rocamora, J. Solís-Guzmán, and M. Marrero. 2016. LCA databases focused on construction materials: A review. *Renewable and Sustainable Energy Reviews* 58 (2016), 565–573. https://doi.org/10.1016/j.rser.2015.12.243

[48] Ange A. Maurice, Khang Ngoc Dinh, Nicolas M. Charpentier, Andrea Brambilla, and Jean-Christophe P. Gabriel. 2021. Dismantling of Printed Circuit Boards Enabling Electronic Components Sorting and Their Subsequent Treatment Open Improved Elemental Sustainability Opportunities. *Sustainability* 13, 18 (2021). https://doi.org/10.3390/su131810357

[49] mblaz. 2019. IO Watch (Arduino IDE Powered Wristwatch) : 8 Steps (with Pictures) - Instructables. https://www.instructables.com/Arduino-Wristwatch/. Accessed: 09-11-2024.

[50] Martin Murer, Anna Vallgårda, Mattias Jacobsson, and Manfred Tscheligi. 2015. Un-Crafting: Exploring Tangible Practices for Deconstruction in Interactive System Design. In *Proceedings of the Ninth International Conference on Tangible, Embedded, and Embodied Interaction* (Stanford, California, USA) *(TEI '15)*. Association for Computing Machinery, New York, NY, USA, 469–472. https://doi.org/10.1145/2677199.2683582

[51] Koya Narumi, Fang Qin, Siyuan Liu, Huai-Yu Cheng, Jianzhe Gu, Yoshihiro Kawahara, Mohammad Islam, and Lining Yao. 2019. Self-healing UI: Mechanically and Electrically Self-healing Materials for Sensing and Actuation Interfaces *(UIST '19)*. Association for Computing Machinery, New York, NY, USA, 293–306. https://doi.org/10.1145/3332165.3347901

[52] Koya Narumi, Xinyang Shi, Steve Hodges, Yoshihiro Kawahara, Shinya Shimizu, and Tohru Asami. 2015. Circuit Eraser: A Tool for Iterative Design with Conductive Ink. In *Proceedings of the 33rd Annual ACM Conference Extended Abstracts on Human Factors in Computing Systems (CHI EA '15)*. Association for Computing Machinery, New York, NY, USA, 2307–2312. https://doi.org/10.1145/2702613.2732876

[53] Marcus Paulo Raele, Lucas Ramos De Pretto, and Denise Maria Zezell. 2017. Soldering mask laser removal from printed circuit boards aiming copper recycling. *Waste Management* 68 (2017), 475–481. https://doi.org/10.1016/j.wasman.2017.07.019

[54] Michael L. Rivera, S. Sandra Bae, and Scott E. Hudson. 2023. Designing a Sustainable Material for 3D Printing with Spent Coffee Grounds. In *Proceedings of the 2023 ACM Designing Interactive Systems Conference* (Pittsburgh, PA, USA) *(DIS '23)*. Association for Computing Machinery, New York, NY, USA, 294–311. https://doi.org/10.1145/3563657.3595983

[55] Rita Shewbridge, Amy Hurst, and Shaun K. Kane. 2014. Everyday making: identifying future uses for 3D printing in the home. In *Proceedings of the 2014 Conference on Designing Interactive Systems* (Vancouver, BC, Canada) *(DIS '14)*. Association for Computing Machinery, New York, NY, USA, 815–824. https://doi.org/10.1145/2598510.2598544

[56] Katherine W Song, Fiona Bell, Himani Deshpande, Ilan Mandel, Tiffany Wun, Mirela Alistar, Leah Buechley, Wendy Ju, Jeeeun Kim, Eric Paulos, Samar Sabie, and Ron Wakkary. 2024. Sustainable Unmaking: Designing for Biodegradation, Decay, and Disassembly. In *Extended Abstracts of the 2024 CHI Conference on Human Factors in Computing Systems (CHI EA '24)*. Association for Computing Machinery, New York, NY, USA, Article 489, 7 pages. https://doi.org/10.1145/3613905.3636300

[57] Katherine W Song, Aditi Maheshwari, Eric M Gallo, Andreea Danielescu, and Eric Paulos. 2022. Towards Decomposable Interactive Systems: Design of a Backyard-Degradable Wireless Heating Interface. In *Proceedings of the 2022 CHI Conference on Human Factors in Computing Systems* (New Orleans, LA, USA) *(CHI '22)*. Association for Computing Machinery, New York, NY, USA, Article 100, 12 pages. https://doi.org/10.1145/3491102.3502007

[58] Katherine W Song and Eric Paulos. 2021. Unmaking: Enabling and Celebrating the Creative Material of Failure, Destruction, Decay, and Deformation. In *Proceedings of the 2021 CHI Conference on Human Factors in Computing Systems (CHI '21)*. Association for Computing Machinery, New York, NY, USA, Article 429, 12 pages. https://doi.org/10.1145/3411764.3445529

[59] Katherine W Song and Eric Paulos. 2023. Vim: Customizable, Decomposable Electrical Energy Storage. In *Proceedings of the 2023 CHI Conference on Human Factors in Computing Systems* (Hamburg, Germany) *(CHI '23)*. Association for Computing Machinery, New York, NY, USA, Article 180, 18 pages. https://doi.org/10.1145/3544548.3581110

[60] Katherine W. Song, Samar Sabie, Steven J. Jackson, Kristina Lindström, Eric Paulos, Åsa Ståhl, and Ron Wakkary. 2025. Unmaking and HCI: Techniques, Technologies, Materials, and Philosophies beyond Making. *ACM Trans. Comput.-Hum. Interact.* 31, 6, Article 76 (Jan. 2025), 6 pages. https://doi.org/10.1145/3689047

[61] Jorge Torrubia, Alicia Valero, and Antonio Valero. 2023. Energy and carbon footprint of metals through physical allocation. Implications for energy transition. *Resources, Conservation and Recycling* 199 (2023), 107281. https://doi.org/10.1016/j.resconrec.2023.107281

[62] Eldy S. Lazaro Vasquez and Katia Vega. 2019. Myco-Accessories: Sustainable Wearables with Biodegradable Materials. In *Proceedings of the 2019 ACM International Symposium on Wearable Computers* (London, United Kingdom) *(ISWC '19)*. Association for Computing Machinery, New York, NY, USA, 306–311. https://doi.org/10.1145/3341163.3346938

[63] Ludwig Wilhelm Wall, Oliver Schneider, and Daniel Vogel. 2023. Substiports: User-Inserted Ad Hoc Objects as Reusable Structural Support for Unmodified FDM 3D Printers. In *Proceedings of the 36th Annual ACM Symposium on User Interface Software and Technology* (San Francisco, CA, USA) *(UIST '23)*. Association for Computing Machinery, New York, NY, USA, Article 34, 20 pages. https://doi.org/10.1145/3586183.3606718

[64] Guanyun Wang, Tingyu Cheng, Youngwook Do, Humphrey Yang, Ye Tao, Jianzhe Gu, Byoungkwon An, and Lining Yao. 2018. Printed Paper Actuator: A Low-Cost Reversible Actuation and Sensing Method for Shape Changing Interfaces. In *Proceedings of the 2018 CHI Conference on Human Factors in Computing Systems* (Montreal QC, Canada) *(CHI '18)*. Association for Computing Machinery, New York, NY, USA, 1–12. https://doi.org/10.1145/3173574.3174143

[65] Shanel Wu and Laura Devendorf. 2020. Unfabricate: Designing Smart Textiles for Disassembly. In *Proceedings of the 2020 CHI Conference on Human Factors in Computing Systems* (Honolulu, HI, USA) *(CHI '20)*. Association for Computing Machinery, New York, NY, USA, 1–14. https://doi.org/10.1145/3313831.3376227

[66] Zeyu Yan, Tingyu Cheng, Jasmine Lu, Pedro Lopes, and Huaishu Peng. 2023. Future Paradigms for Sustainable Making. In *Adjunct Proceedings of the 36th Annual ACM Symposium on User Interface Software and Technology* (San Francisco, CA, USA) *(UIST '23 Adjunct)*. Association for Computing Machinery, New York, NY, USA, Article 109, 3 pages. https://doi.org/10.1145/3586182.3617433

[67] Zeyu Yan, Mrunal Dhagude, and Huaishu Peng. 2025. Make Making Sustainable: Exploring Sustainability Practices, Challenges, and Opportunities in Making Activities *(CHI '25)*. Association for Computing Machinery, New York, NY, USA. https://doi.org/10.1145/3706598.3713665

[68] Zeyu Yan, Jiasheng Li, Zining Zhang, and Huaishu Peng. 2024. SolderlessPCB: Reusing Electronic Components in PCB Prototyping through Detachable 3D Printed Housings. In *Proceedings of the CHI Conference on Human Factors in Computing Systems (CHI '24)*. Association for Computing Machinery, New York, NY, USA, Article 345, 17 pages. https://doi.org/10.1145/3613904.3642765

[69] Zeyu Yan, Anup Sathya, Sahra Yusuf, Jyh-Ming Lien, and Huaishu Peng. 2022. Fibercuit: Prototyping High-Resolution Flexible and Kirigami Circuits with a Fiber Laser Engraver. In *Proceedings of the 35th Annual ACM Symposium on User Interface Software and Technology* (Bend, OR, USA) *(UIST '22)*. Association for Computing Machinery, New York, NY, USA, Article 12, 13 pages. https://doi.org/10.1145/3526113.3545652

[70] Lan Yin, Huanyu Cheng, Shimin Mao, Richard Haasch, Yuhao Liu, Xu Xie, Suk-Won Hwang, Harshvardhan Jain, Seung-Kyun Kang, Yewang Su, Rui Li, Yonggang Huang, and John A. Rogers. 2014. Dissolvable Metals for Transient Electronics. *Advanced Functional Materials* 24, 5 (2014), 645–658. https://doi.org/10.1002/adfm.201301847

[71] Zhihan Zhang, Agni K Biswal, Ankush Nandi, Kali Frost, Jake A Smith, Bichlien H Nguyen, Shwetak Patel, Aniruddh Vashisth, and Vikram Iyer. 2024. Recyclable vitrimer-based printed circuit boards for sustainable electronics. *Nature Sustainability* 7, 5 (May 2024), 616–627. https://doi.org/10.1038/s41893-024-01333-7

[72] Zhihan Zhang, Felix Hähnlein, Yuxuan Mei, Zachary Englhardt, Shwetak Patel, Adriana Schulz, and Vikram Iyer. 2024. DeltaLCA: Comparative Life-Cycle Assessment for Electronics Design. *Proc. ACM Interact. Mob. Wearable Ubiquitous Technol.* 8, 1, Article 29 (mar 2024), 29 pages. https://doi.org/10.1145/3643561

[73] Junyi Zhu, Lotta-Gili Blumberg, Yunyi Zhu, Martin Nisser, Ethan Levi Carlson, Xin Wen, Kevin Shum, Jessica Ayeley Quaye, and Stefanie Mueller. 2020. CurveBoards: Integrating Breadboards into Physical Objects to Prototype Function in the Context of Form. In *Proceedings of the 2020 CHI Conference on Human Factors in Computing Systems* (Honolulu, HI, USA) *(CHI '20)*. Association for Computing Machinery, New York, NY, USA, 1–13. https://doi.org/10.1145/3313831.3376617

[74] Jingwen Zhu, Lily Winagle, and Hsin-Liu (Cindy) Kao. 2024. EcoThreads: Prototyping Biodegradable E-textiles Through Thread-based Fabrication. In *Proceedings of the CHI Conference on Human Factors in Computing Systems* (Honolulu, HI, USA) *(CHI '24)*. Association for Computing Machinery, New York, NY, USA, Article 857, 17 pages. https://doi.org/10.1145/3613904.3642718